Long-Term Support
World Class Quality

New Serial RAM Products

SPI RAM

Features:

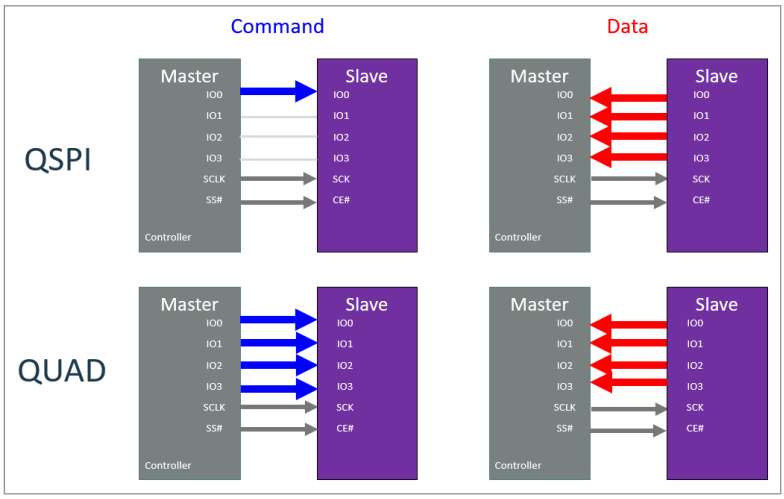
- Densities: 8Mb, 16Mb, 32Mb
- Voltage:
  2.7~3.6 & 1.65~1.95V
- SPI and QPI Compatible Interface:
  SPI (x1), SQI (x4)
  QPI Default Option available
- 32 byte and 1024 byte Wrapped Burst Operation for Reads and Writes
- Continuous operation only option available
- Automotive Grade Available
- Temperature Supported: -40 to 85°C; -40 to 105°C
- Speed: SPI/QSPI: 104MHz
- Max Bandwidth: 52MB/s
- Packages: 8-Pin SOIC, 8-Pin WSON, WLCSP
- Samples: Available Now

QUAD RAM

Features:

- Densities: 8Mb, 16Mb, 32Mb
- Voltage and Speed:
  2.7~3.6 (up to 133MHz)
  1.7~1.95V (up to 200MHz)
- JEDEC standard Quad I/O with DS NOR Flash Compatible Interface (4S-4D-4D)
- Max Bandwidth: 200MB/s
- Low Signal Counts: 7 Signal pins (CS#, SCLK, DQSM, SIO0~SIO3)
- Source Synchronous Output signal during Read operation (DQSM)
- Data Mask during Write operation (DQSM)
- Hardware RESET (RESET#) and JEDEC Standard In-Band Reset operation
- Fixed Latency Mode and Variable Latency Mode
- On Chip ECC (2D1C)with optional ERR signal in 8Mb/16Mb
- Automotive Grade Available
- Temperature Supported: -40°C to 85°C; -40°C to 105°C; -40°C to 125°C (8Mb, 16Mb)
- Packages: 24-ball BGA: 200MHz; 16-pin SOIC: 133MHz, WLCSP
- Samples: Available Now

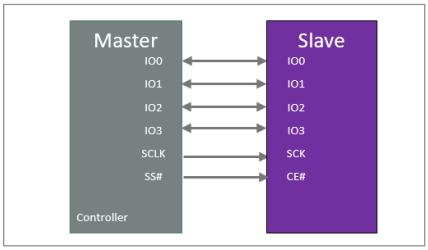
QSPI vs QUAD



Quad SPI (QSPI) and QUAD Notation

SPI Protocols	CMD	Address	Data	Notation
Standard SPI	1 pin	1 pin	1 pin	1/1/1
QSPI (Quad SPI)	1 pin	4 IO pins	4 IO pins	1/4/4
QPI	4 IO pins	4 IO pins	4 IO pins	4/4/4

Connection Diagram



	SPI RAM	QUAD RAM
Densities	8Mb, 16Mb, 32Mb	8Mb, 16Mb, 32Mb
Packages	8-Pin SOIC, 8-Pin WSON, WLCSP	24-ball BGA: 200MHz; 16-pin SOIC: 133MHz, WLCSP
Temperature Supported	-40°C to 85°C; -40°C to 105°C	-40°C to 85°C; -40°C to 105°C; -40°C to 125°C (8Mb, 16Mb)
ECC	Not Supported	On Chip ECC (2D1C)with optional ERR signal in 8Mb/16Mb
Speed	SPI/QSPI: 104MHz	2.3~3.6 (up to 133MHz) 1.65~1.95V (up to 200MHz)

ADDITIONAL FAQs

- **Q: What is variable latency and fixed latency?**
  Variable Latency:
  An additional latency during read/write operation is added to the initial latency when a refresh collision occurs.
  Fixed Latency:
  The latency is always fixed during read/write operation regardless of refresh collision.

- **Q: What is the difference between Wrap Burst Operation and Continuous Operation?**
  Wrap burst has pre-defined length, such as 16,32,64 and 128.
  Continuous Operation is for the entire chip. After the end of the memory array is reached, it goes back the first byte of the memory array of the chip.

- **Q: Data Rate Difference between SerialRAM and QUADRAM:**
  SerialRAM: Address and Data are always SDR
  QUADRAM: Address and Data are always DDR

- **Q: How does DQSM work?**
  DQSM offers two different functions based on the operating mode.
- When the device is in a read operation, the DQSM signal becomes driven by OctalRAM/QUADRAM to indicate the data output. This signal is synchronized with data output. (within tDQSQ) The controller uses this signal to adjust the referencing time of data output to maximize the data eye and minimize the variation by temperature, voltage, and sample variation. And this signal will have a latency depending on the refresh event. If the variable refresh option is used, this signal must be monitored to avoid the refresh collision.
- When the device is in a write operation mode, the DQSM becomes an input pin and the device uses it for masking data inputs. DQSM high means the data is masked and 8 bits of data inputs at the clock edge won't be written into OctalRAM/QUADRAM. The OctalRAM/QUADRAM uses a serial protocol sharing IO pins for command and address inputs. Maximizing data throughput will be shown in a continuous or burst mode. By using the data mask feature, the user continuously uses the same address and command to deploy the necessary data to be updated.