

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

Practical guidelines to get the best operation of HV and MV CoolGaN™

## About this document

### Scope and purpose

The fast-switching capability of HV and MV GaN transistors makes PCB layout challenging. This application note discusses several key concepts to help users understand the layout challenges and strategies to help optimize the layout for the best overall electrical and thermal performance in switched-mode power supplies (SMPS) applications.

### Intended audience

SMPS design engineers, PCB layout engineers, technicians, and developers of electronic systems interested in the optimal performance achievable with HV and MV GaN devices.

### Keypoints

- PCB layout design challenges in high-frequency applications
- Managing and optimizing parasitic impedances in PCB layouts
- Optimizing parasitic inductance, thermal management, heat dissipation, and layout for improved performance

## About this product family

### Product family

Infineon's CoolGaN™ product family offers a range of power transistors offering a versatile and scalable solution for consumer and industrial applications. With a broad voltage range of 60 V to 700 V and various packages, they offer superior switching speed, high-power density, and reduced energy losses, resulting in smaller, lighter, and more compact systems with improved reliability and thermal conductivity. With their higher thermal conductivity and robust design, they are capable of withstanding high voltage spikes and ensuring a longer lifespan, making them an ideal choice for designers seeking to create innovative and efficient power management solutions.

### Target applications

- [Server power supply units \(PSU\)](#)
- [Telecom SMPS](#)
- [Adapters and chargers](#)
- [LED lighting system design](#)
- [Home appliances](#)
- [Complete system solutions for smart TVs](#)

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications



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### Introduction

## 1 Introduction

PCB layout has been an integral aspect of power electronic design since the first switching power supplies appeared more than 40 years ago. Regardless of the transistor technology, the parasitic impedances added to the circuit by the PCB layout must be understood and managed for the circuit to function correctly, reliably, and without causing undue electromagnetic interference (EMI).

Even though modern wide-bandgap power semiconductors do not suffer the severe reverse-recovery problems of legacy silicon technologies, their much faster switching transitions result in even more extreme commutation  $dv/dt$  and  $di/dt$  than their silicon predecessors. The common advice offered by generic application notes on power electronic PCB layout is to “minimize parasitic inductance as much as possible”. However, the best way to do that is not always clear. Moreover, not all conductive paths necessarily need to be the lowest possible inductance: consider the interconnection to an inductor – naturally, there will already be inductance in that path.

It is of course impossible to minimize all interconnection inductance and simultaneously eliminate all node-to-node capacitance on a PCB. The key to successful PCB layout is therefore to understand where the impedances really matter in switched-mode power electronics, and how to mitigate any undesired consequences of this inevitable impedance.

An additional complicating factor is that PCB layout not only involves optimizing the electrical interconnection but often requires thermal pathways that conflict with electrical optimization goals. Even mechanical structures like heatsinks, when applied to the PCB and separated only by a thin thermal interface material (TIM), can behave like an additional electrical plane of the PCB assembly, and interact with the switching nodes of the circuit.

This application note begins by explaining the fundamentals: what really happens during a switching transition, what is the cause versus effect of the transient voltages and currents we see, and where exactly the current is flowing. When we think about current flow, we often forget to consider the return path, which is critically important. An additional key concept is how we think about inductance: it is often viewed as individual inductive elements that all add up around a loop. But they don't necessarily all add up: depending on the geometric relationship between source and return current, the mutual inductance can change the sign, resulting in subtraction rather than addition. The concepts of loop, partial, and mutual inductance help us to explain and understand this interaction.

Next, different power-stage layout options are presented, along with the tradeoffs involved with each. The overall goal here is to understand the best ways to minimize power-loop inductance. With traditional through-hole transistors mounted perpendicular to the PCB, the inductance of the transistor package is independent of the PCB layout because they are at right angles. For SMT packages, the package inductance itself is a function of how the return path is routed, so there are more layout options and alternatives to improve overall performance.

Since design of the power loop includes thermal as well as electrical path optimization, the options and tradeoffs of top versus bottom-side cooled transistor packages are covered. Finally, the design, layout, and routing of the gate driver circuit, along with its “hidden” current paths, are explained.

### The practical problem

## 2 The practical problem

The physical layout and packaging of power electronic circuits adds “parasitic” circuit elements  $R_{\text{Parasitic}}$ ,  $C_{\text{Parasitic}}$ , and  $L_{\text{Parasitic}}$ . These parasitic elements can cause unexpected behavior and unintended consequences, circuit malfunction, EMI, oscillations and, in severe cases, cross-conduction or “shoot-through” that can lead to transistor failures. Resistive parasitics are comparatively easy to understand – especially for DC current. The solution to minimize parasitic resistance is to use more copper – to increase the total current-carrying cross-section. With high-frequency AC currents, the situation is more complex due to the skin effect. For PCB-integrated magnetics, the skin and proximity effects need to be carefully considered, but that is outside the scope of this document.

The concept of parasitic capacitance is also straightforward. Especially in a structure like a PCB, where the copper layers form parallel plates with thin dielectric layers in between. We can use simple 2D tools to estimate the  $C \approx \epsilon_0 \epsilon_R \left( \frac{\text{area}}{\text{spacing}} \right)$  and we can easily estimate capacitance per area for a given layer stackup. As we will see later, sometimes the capacitive coupling paths comprise components rather than the PCB itself. The question of which capacitance value is acceptable will be covered later as well.

Parasitic inductance is different: basic circuits classes teach us to think of inductors as discrete elements that sum like resistors in series. However, in more advanced magnetics courses, we learn that they interact with each other through mutual inductance, which can either increase or decrease the total inductance, depending on the geometry and direction of current flow. Also, we often don’t have a good estimate of layout inductance, or know the magnitude of  $di/dt$  to expect from our switching circuit – how much will cause problems?

These layout issues are not new to power electronics, but GaN transistors with low charge and no reverse recovery make switching transitions even shorter. Fast-switching transistors primarily cause two interrelated issues. The high transconductance of GaN, combined with its low gate charge, can result in very high  $(di_{DS})/dt$ , in the range of about 2 to 20 A/ns, which will lead to larger transient voltage across any parasitic inductance. In addition, the low output charge results in a very fast  $(dV_{DS})/dt$ , which can exceed 100 V/ns.

Why are fast  $dI/dt$  and  $dV/dt$  problematic? On the one hand, fast turn-on  $dI/dt$  reduces switching time and therefore loss, so it should be desirable. But the problems that occur are primarily due to the  $L dI/dt$  reaction voltage that appears across parasitic inductive elements. Most commonly the undesirable effects occur in the main commutation loop, and also in the gate driver loop. Voltage overshoot in the power loop can increase EMI issues and create HV stress on the transistors, leading to reduced reliability. In the gate loop,  $L dI/dt$  reaction voltage will slow switching speed by subtracting from the applied gate voltage but can also lead to ringing and overshoot of  $V_{GS}$ , or even oscillatory behavior, which can quickly destroy the transistor.

These key concepts – optimizing the commutation-loop and the gate driver layout including both the turn-on and turn-off loops, combined with shielding capacitive currents from disrupting the gate driver – will be covered in detail with examples in the following sections.

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

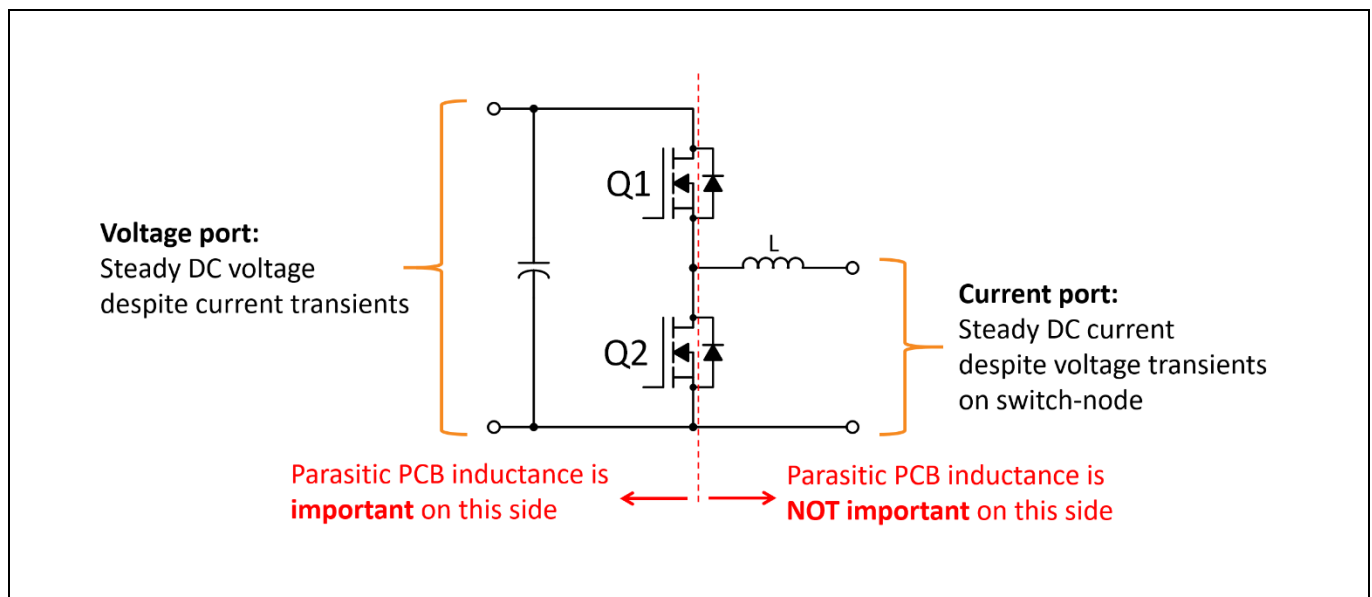
## Practical guidelines to get the best operation of HV and MV CoolGaN™

### A detailed look at the half-bridge in hard switching

## 3 A detailed look at the half-bridge in hard switching

The half-bridge topology is widely used configuration in power electronics. It is the basis of “totem-pole” bridgeless power-factor correction (PFC), full-bridge DC-DC converters, LLC converters, inverters, and many others. Simply put, the half-bridge topology is a two-port network, as shown in [Figure 1](#). GaN in half-bridge topology is an ideal transistor candidate due to its low output charge and no body-diode recovery, which makes them interchangeable in both hard- or soft-switching applications.

The left side of the circuit is a voltage port that represents a DC bus. The DC bus voltage should remain steady despite the current transients that occur when the transistors switch. It doesn't matter if the power flow is to the left or right; in either case, the bus should remain fixed. The right-hand side of the circuit is a current port. Here, the inductor current should remain steady despite the voltage transients on the switch-node. This is an important distinction, because it indicates that parasitic inductance is important for the loop on the left side – to minimize  $L \frac{dI}{dt}$  transient voltages from appearing across the transistors. But the right side is already an inductive path – so here it really doesn't matter if some extra parasitic inductance is added – it will be insignificant compared to the intended inductor.



**Figure 1** Half-bridge topology is a two-port network; parasitic inductance is important on the voltage port

Another useful concept to help understand switching behavior is to think about what the forcing function is. Rapidly changing currents cause a reaction voltage  $v = L \frac{dI}{dt}$ , and rapidly changing voltage induces current  $i = C \frac{dV}{dt}$ , but which is the cause versus effect? For hard-switching transistors, current is the forcing function. During switching, the transistor acts as a transconductance amplifier – driving current in response to the gate signal. How quickly the transistor turns on ( $\frac{dI}{dt}$ ) is limited by how quickly the gate can be fully enhanced.  $\frac{dV}{dt}$ , on the other hand, is an effect: it is the result of how rapidly the applied current can charge the node capacitances.

Now consider the switching transients in the half-bridge. [Figure 2](#) shows a half-bridge setup for pulse testing: Q2 is the active switch, and Q1 serves as a synchronous rectifier. The switching diagram shows the hard-switched turn-on of Q2, followed by its turn-off (which is essentially zero-voltage switching, ZVS). This emulates

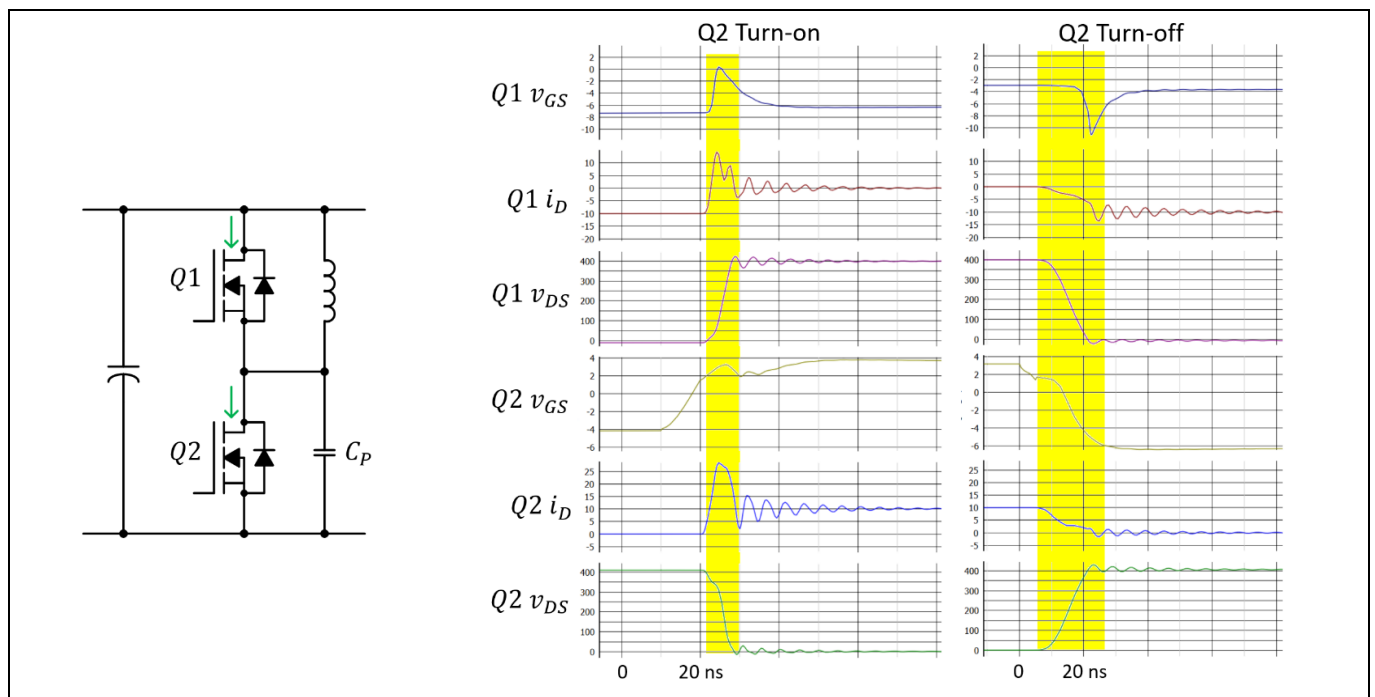
# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

## Practical guidelines to get the best operation of HV and MV CoolGaN™

### A detailed look at the half-bridge in hard switching

the typical circuit operation of a totem-pole PFC operating in continuous conduction mode (CCM). In both cases, the initial inductor current is 10 A, and the bus voltage is 400 V.

Note that when Q2 turns on, its drain current far surpasses the 10 A inductor current, peaks at 28 A, then returns and settles down to the 10 A inductor current after the resonances damp-out. This waveform looks suspiciously like reverse recovery, but the key is to look at the timing of  $v_{DS}$  versus  $i_D$ . Reverse recovery prevents the high-side diode (Q1) from blocking voltage – so it essentially remains on (conducting), until the peak of the  $i_D$  waveform – then  $v_{DS}$  begins to change. That is the classic signature of reverse recovery. But here,  $v_{DS}$  is clearly beginning to move as soon as the drain current exceeds the inductor current, indicating that the response is purely capacitive with no reverse recovery.



**Figure 2** Hard-switched turn-on and turn-off of a GaN half-bridge

The area under the 28 A peak, above the 10 A inductor current line, represents the charge that Q2 has to discharge. It is the sum of Q1's  $Q_{OSS}$  plus the parasitic PCB capacitance represented by  $C_p$ . These currents are very difficult to accurately measure on the PCB unless a dedicated wide-bandwidth current-shunt is added to the circuit. Here we use simulation to estimate the current, and a value for  $C_p$  is added to the simulation circuit. But even with this simulation, what we do not see is the internal self-discharge current of Q2's  $Q_{OSS}$ . While it does contribute to hard-switched losses, the discharge path is entirely contained on the transistor die, so the effect of this added capacitive current is not seen in the PCB layout.

*Note: The transient current during switching is difficult to measure, and simulation requires adding accurate parasitic elements. In this case, the peak current is 18 A above inductor current, and the slew rate is about 9 A/ns at turn-on. This represents a typical value measured on dedicated GaN test setups and characterization platforms, where the turn-on  $\frac{di}{dt}$  is typically measured in the range from 4 to 16 A/ns. This typical value will be used in various layouts to assess what the resulting transient voltages could be.*

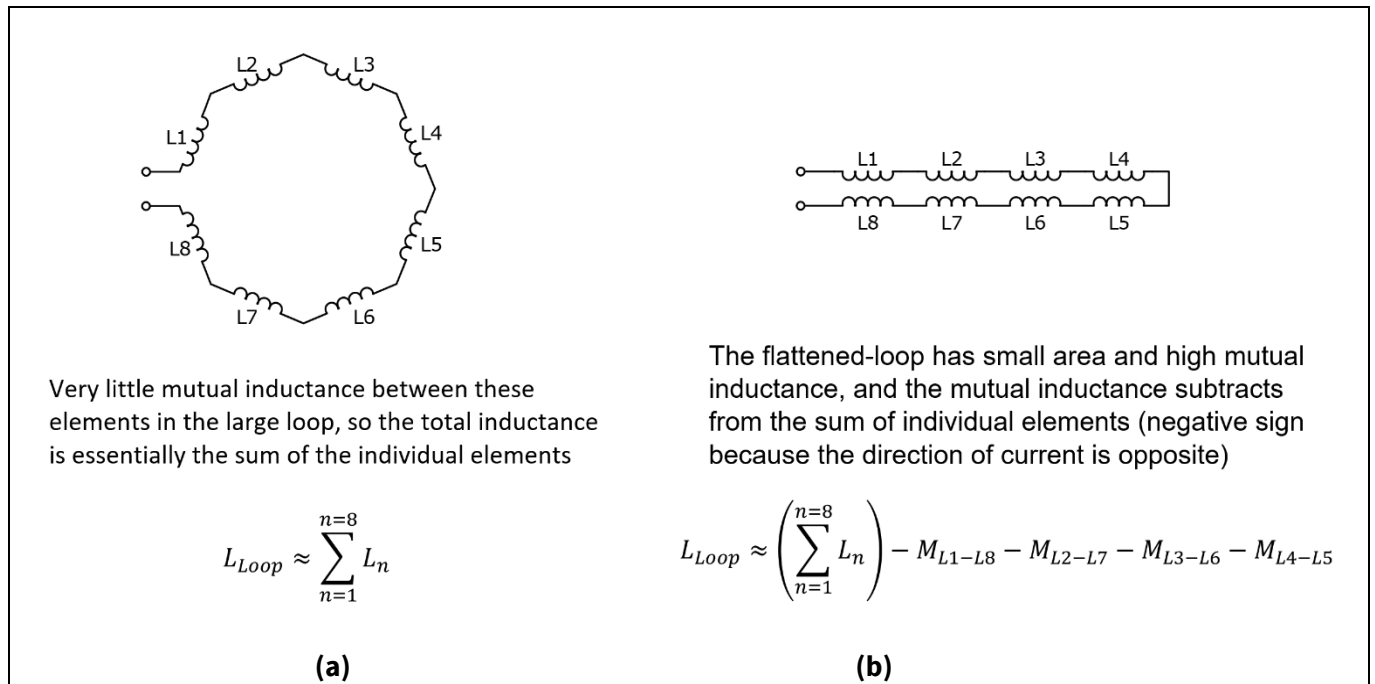
# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

## Practical guidelines to get the best operation of HV and MV CoolGaN™

### Mutual and partial inductance

## 4 Mutual and partial inductance

Before addressing how to minimize parasitic inductance on a PCB layout, a few inductance concepts will be reviewed. Consider a piece of wire formed into a single-layer loop 100 mm in diameter. Measuring the inductance of that loop with an impedance analyzer would indicate about 250 nH. You could make a piecewise linear model of this by connecting ‘n’ number of small inductors in series around a loop, as shown in [Figure 3a](#).



**Figure 3 a) Model of inductances around a circular loop; b) the same loop, flattened**

In this example, n = 8 is considered for simplicity. Knowing that inductors in series sum just like resistors, each of the eight elements represents a 31 nH segment of the circle. This does not hold true if we take the same piece of wire and flatten out the loop as shown in [Figure 3b](#): now the measured inductance drops to a much smaller value.

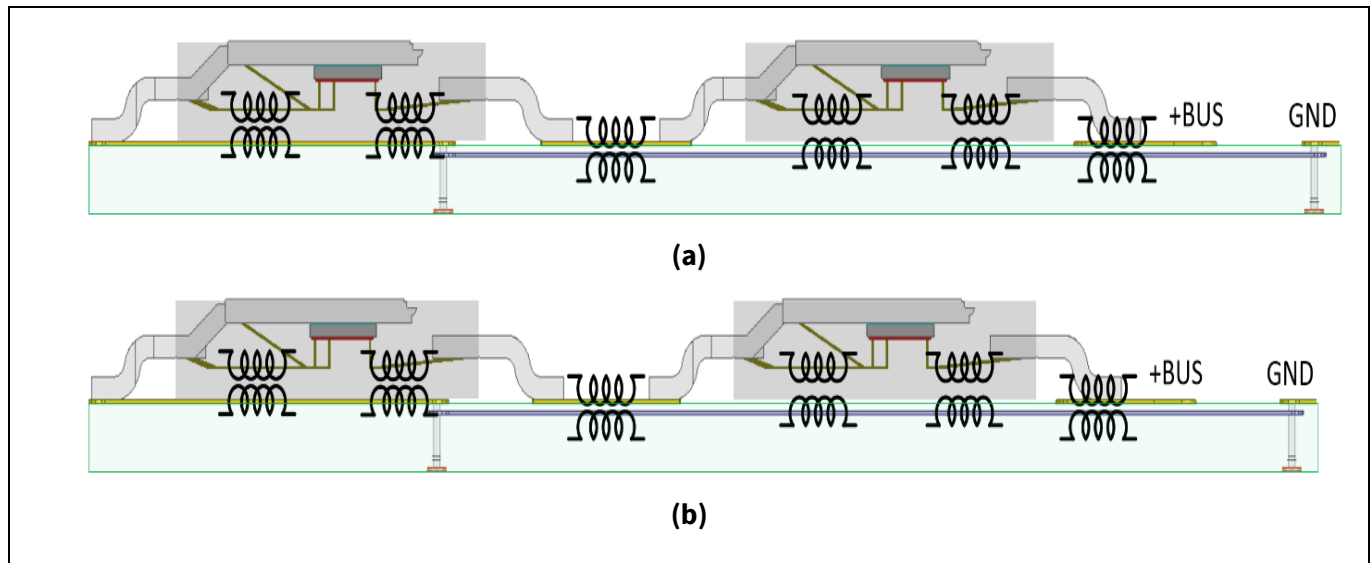
The change is explained by the concept of partial inductance [1]. The value of each segment  $L_n$  is equal to its *intrinsic* inductance in free space (its partial inductance), plus the effect of mutual inductance (M) from nearby segments. Note that mutual inductance has both magnitude and sign, so it can add to or subtract from the intrinsic inductance. In the example of [Figure 3b](#), the direction of current flow in L1 and L8 is opposite, thus the mutual inductance subtracts from the partial inductance of each segment. The same holds true for all pairings shown. Power electronic engineers commonly think about mutual inductance when specifically designing a transformer, for example, but it may not be as obvious when simply thinking about conductive tracks on a PCB.

Another equally valid way to consider round versus flat-loop inductance change, as shown in [Figure 3](#), is to apply Ampere’s law and note that the loop *area* has been reduced, and thus the flux linked is also reduced, leading to the inductance reduction. These are simply two different ways to think about the same situation, and both are valid.

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

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## Mutual and partial inductance



**Figure 4** a) Power loop with narrow spacing between layers maximizes mutual inductance, b) Increased layer spacing reduces mutual inductance, resulting in a higher overall total commutation loop inductance

Now, consider the same wire loop experiment in the context of a PCB layout, as shown in [Figure 4a](#). The loop begins at Cbus+ and ends at Cbus- (the power commutation loop). The individual inductive elements represent the wire bonds in the transistor package, the leadframe, copper segments on the PCB, and so on. Comparing the two different layer spacings shown in [Figure 4a](#) and [Figure 4b](#), it should be clear that the mutual inductance will be greatest when the spacing between the surface current and the return path current is smallest. This is also consistent with the smallest loop area.

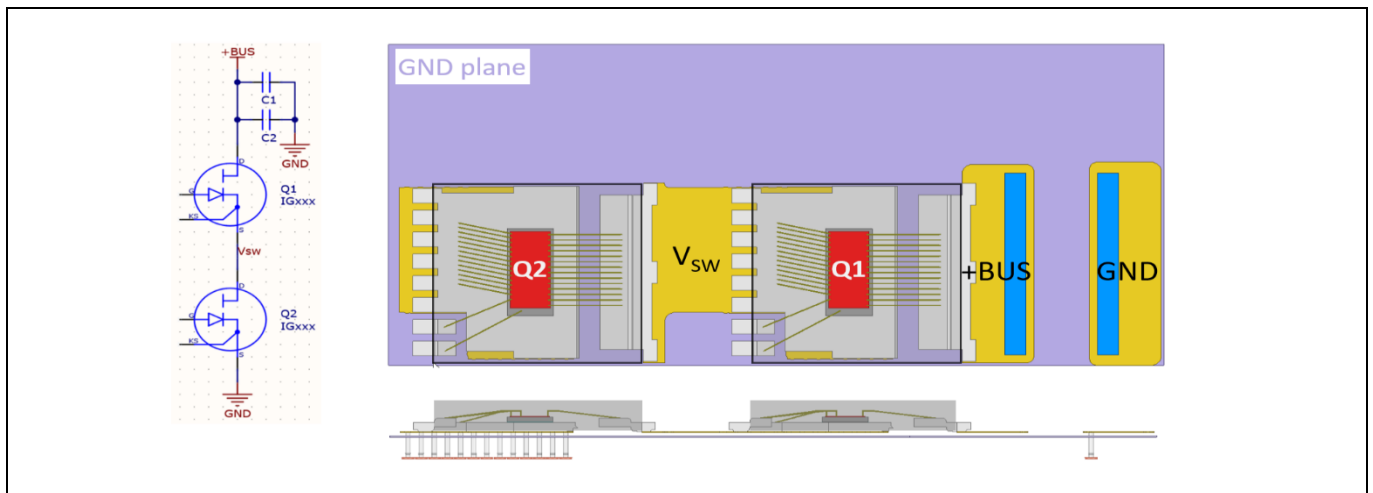
# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

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Package inductance: Is it a fixed value, or layout dependent?

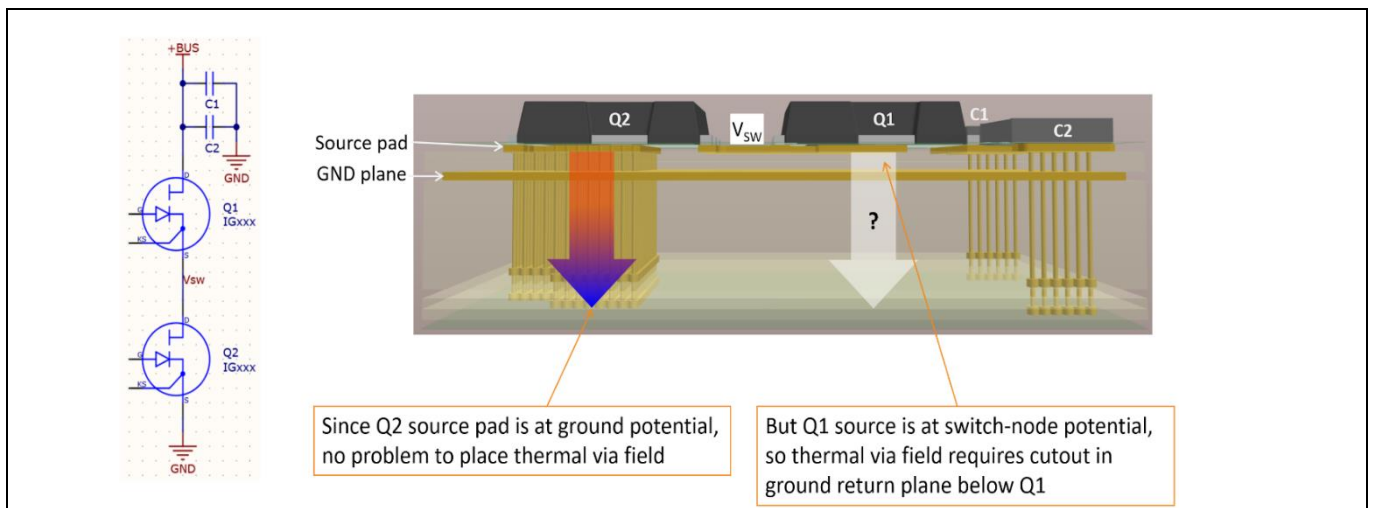
## 5 Package inductance: Is it a fixed value, or layout dependent?

Generally, the calculated transistor package inductance is simply the partial inductance — no mutual inductance is presumed external to the package. In other words, the specified package inductance assumes the return-path is infinitely far away and does not affect the partial inductance. For through-hole packages like the TO-220 and TO-247, this assumption is valid, since the package is commonly mounted perpendicular to the PCB and the current paths are orthogonal, thus no mutual inductance. But for surface-mounted packages, an optimized current return-path will significantly reduce the effective inductance of the in-situ package.



**Figure 5** Low commutation-loop inductance using surface-mounted “TOLL”-packaged GaN transistors,  $L = 2.8 \text{ nH}$

To illustrate this, consider a simple half-bridge layout as shown in Figure 5. The commutation loop runs from the +BUS pad, through Q1 and Q2, from right-to-left through the transistor packages and on the surface layer (gold color). Then the current drops to the second layer (violet color) through vias below Q2 source. The return current then flows in the opposite direction back to the GND on the far right. This is like the flattened loop as shown in Figure 3b, where each of the parasitic inductances (a bondwire, for example) has a corresponding segment in the ground return plane.



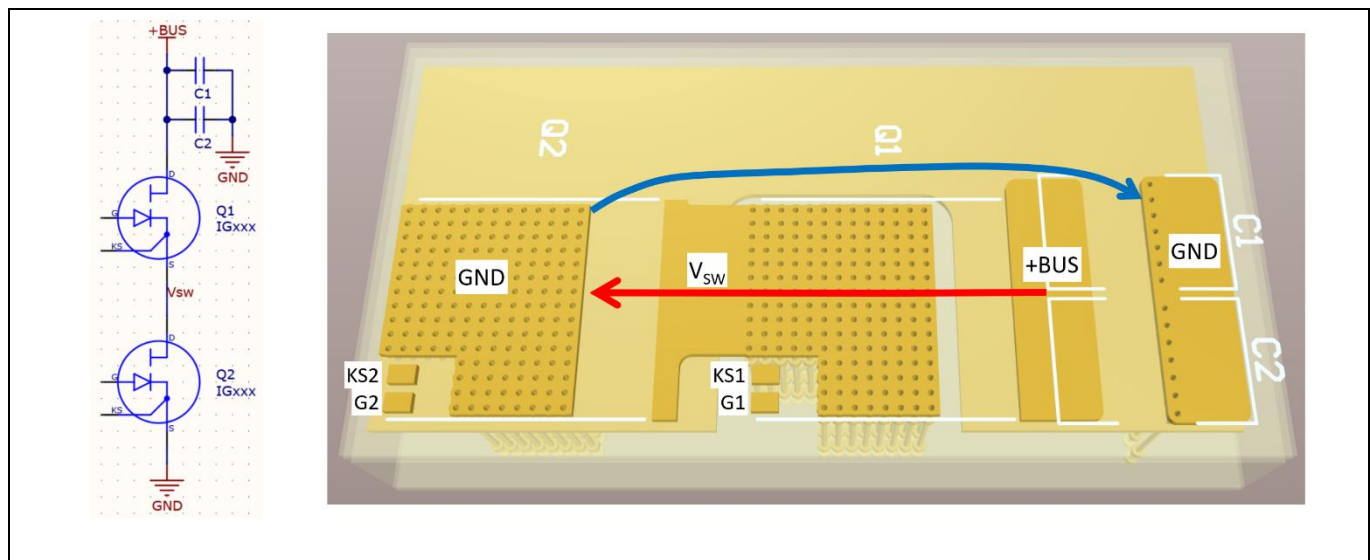
**Figure 6** Need for the Q1 thermal path will make optimal electrical layout challenging

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

## Practical guidelines to get the best operation of HV and MV CoolGaN™

### Package inductance: Is it a fixed value, or layout dependent?

The mutual inductance (or small loop area) makes the total loop inductance quite small. In fact, using 3D Finite Element Analysis, the calculated loop inductance of the geometry shown is only 2.8 nH. This seems impossibly small, since the total package inductance in the transistor models shows 2.1 nH per transistor. This is a perfect example of how the package partial inductance can be misleading, because it ignores the effect of the return path as discussed earlier. The explanation is that the 2.1 nH package inductance is reduced by the mutual inductance of the return path when laid out as shown here. While the loop inductance of this example is impressively low, there is a fundamental problem in trying to use this layout in a real power converter: there is no space to insert a thermal via field to remove heat from Q1 without creating a big hole in the ground return path under Q1. [Figure 6](#) illustrates the problem.



**Figure 7** Ground-plane clearance around the via field creates a lateral loop in return path,  $L = 8.8$  nH

Adding a cutout for thermal vias will redirect the return current under Q1, and this will not only reduce the mutual inductance, but it will create a lateral loop with additional inductance. [Figure 7](#) shows the addition of the thermal via field, and the cutout necessary for clearance around the voltage of the switch-node.

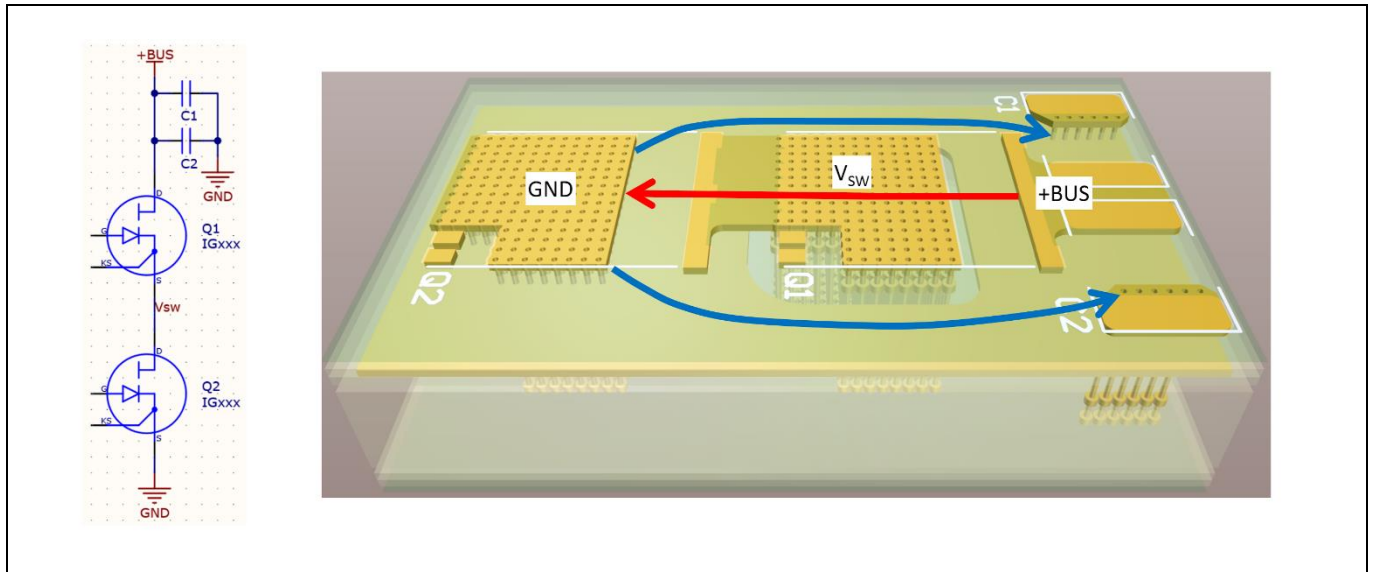
The current path through the transistors (in red) is essentially the same as before. But now, the ground return path (in blue) is not directly below the red path. As a result, a lateral loop is formed, which reduces mutual inductance and increases the total loop inductance. When comparing the two layouts, a notable increase in loop inductance is observed with the addition of the cutout. Specifically, the loop inductance in [Figure 5](#) is 2.8 nH, whereas in [Figure 7](#), it increases to 8.8 nH, almost triple the value.

The “single-sided return” in [Figure 7](#) does leave the gate pads (G1 and KS1) open and easy to connect on either side of the PCB. What if a second, parallel ground return-path were added on the gate side of the transistors? This example is shown in [Figure 8](#). Now, there are two lateral loops in parallel, so the parallel combination should reduce the lateral-loop inductance—and it does. The “double-sided return” path of [Figure 8](#) has a total loop-inductance of 6.2 nH. This is still more than double compared to [Figure 5](#), but a significant improvement over the single-sided return-path.

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

Practical guidelines to get the best operation of HV and MV CoolGaN™

Package inductance: Is it a fixed value, or layout dependent?



**Figure 8** Double-sided return path around the thermal via field significantly reduces lateral loop inductance,  $L = 6.2 \text{ nH}$

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

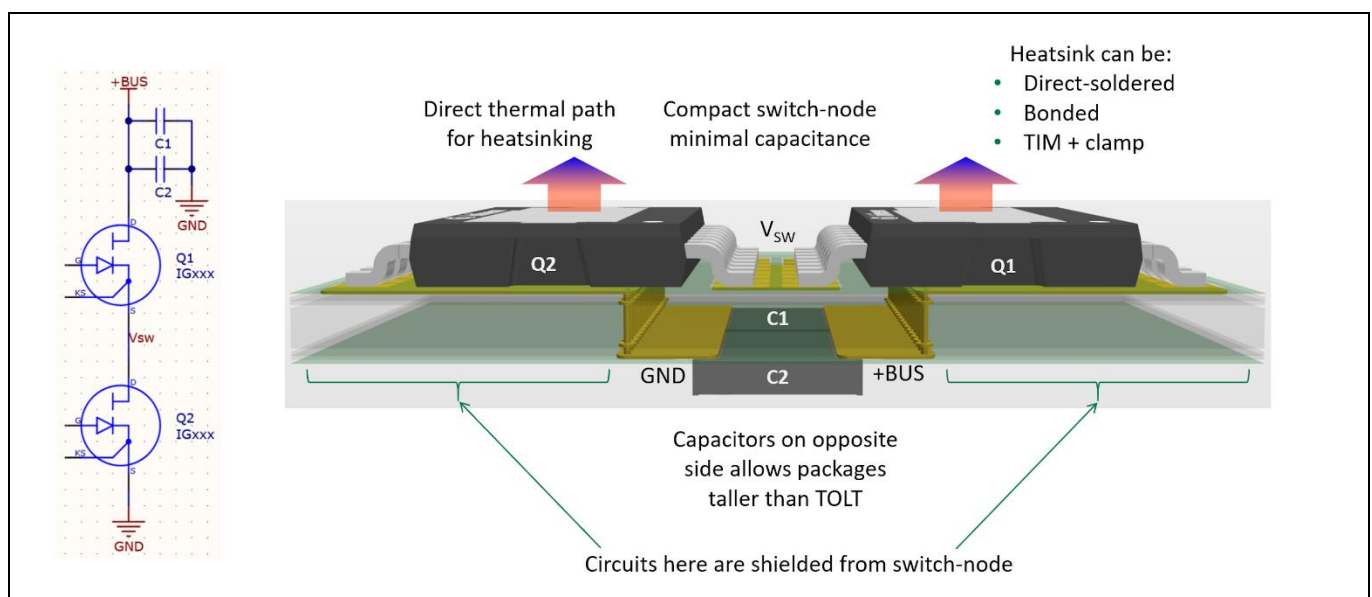
## Practical guidelines to get the best operation of HV and MV CoolGaN™

### Advantage of topside-cooled transistor packages

## 6 Advantage of topside-cooled transistor packages

The previous layout options using bottom-side cooled packages all require compromises in electrical layout to accommodate the thermal vias necessary to remove heat from the transistor(s). Adding 100 or more thermal vias per transistor not only compromises the electrical layout, but vias cost money: every drill operation (especially for small-diameter drills) adds cost to the PCB manufacturing process.

Another option to consider is using topside-cooled transistor packages. Sometimes, these are simply the same bottom-side cooled devices with a flipped lead-bend. But in most cases, the topside-cooled transistors are packages specifically designed to optimize both thermal and electrical performance of GaN transistors. [Figure 9](#) shows an example of the same half-bridge layout, but this time using a TOLT package.



**Figure 9 Top-side cooled transistors enable optimization of both electrical and thermal paths, resulting in 5.8 nH loop inductance**

The big difference here is that, compared to the previous layouts, there are NO thermal via fields required below the transistors. This saves cost and allows electrical layout optimization *independent* of the thermal path. An additional benefit is that the ground and +BUS planes, which are electrically “quiet” equipotential planes, serve as Faraday shields between the noisy switch-node and any other circuits on the bottom-side of the board.

In this example, the high-frequency bus capacitors C1 and C2 are located on the bottom-side of the board. This is sometimes necessary, depending on the height of the capacitors and the geometry of the heatsink, to avoid interference and enable proper creepage and clearance for the heatsink on top of the transistors. Although, this option does leave loop area above the capacitors that increases commutation loop inductance, using a thinner board (0.8 mm versus 1.6 mm thick, for example) will reduce that.

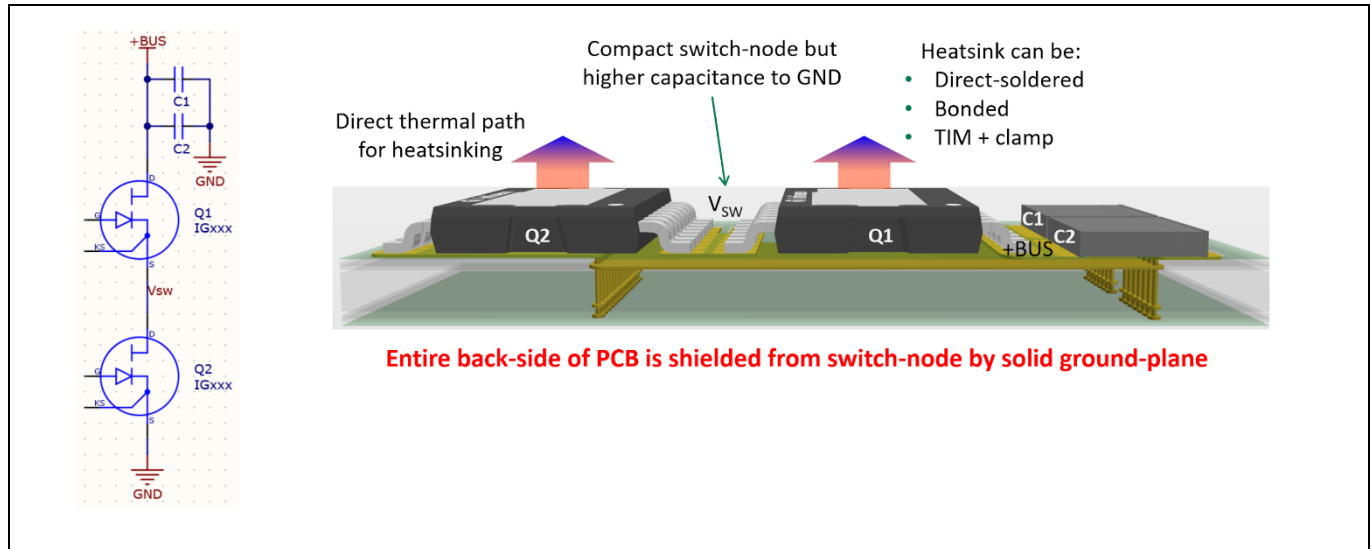
As another option, if there is room to locate C1 and C2 on the same side of the PCB as the transistors, then the layout in [Figure 10](#) can provide an excellent low-inductance commutation loop. Even though the return path is extended longer than [Figure 9](#) laterally, the spacing between layers is much thinner (0.18 mm, for example), making the overall commutation loop even better than [Figure 9](#). An additional benefit of the layout in [Figure 10](#) is that the entire bottom-side of the PCB is electrically “quiet” – it is shielded from the switch-node on the top

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

## Practical guidelines to get the best operation of HV and MV CoolGaN™

### Advantage of topside-cooled transistor packages

of the board. This frees up more area on the bottom for other circuits and helps to improve overall power density.



**Figure 10** Moving the capacitors to the same side as the transistors for lowest overall inductance with top-side cooled devices, providing 4.9 nH loop inductance

The example top-side cooled packages shown here do not have an electrically isolated “heatslug”: the metal pad itself is a part of the leadframe, so it is electrically connected to the source potential. As the metal is solderable, individual copper heatsinks could be directly soldered to each transistor. Alternatively, thermal interface materials can be used with many other heatsink options as well.

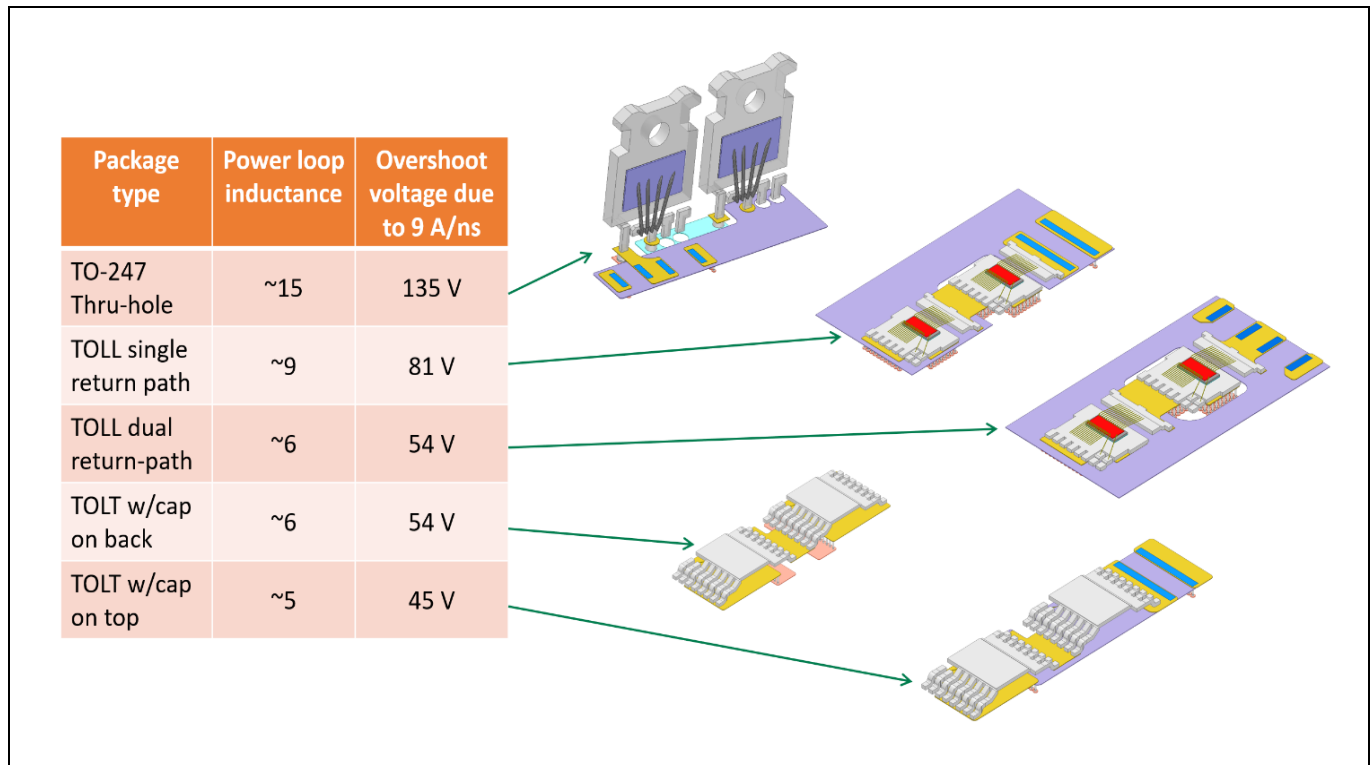
# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

## Practical guidelines to get the best operation of HV and MV CoolGaN™

### Summary of commutation-loop layout options and results

## 7 Summary of commutation-loop layout options and results

All of these SMT layout options can be compared to a standard TO-247 package to see the overall loop inductance and estimate what the overshoot voltage would be for a half-bridge assuming  $9 \text{ A/ns } \frac{di}{dt}$ , as previously discussed. The best-case TO-247 layout results in about 15 nH of total loop inductance, as shown in [Figure 11](#).



**Figure 11 Summary of power-loop inductance and implications**

Applying this knowledge to the expected  $di/dt$ , we see that the resulting overshoot voltage would peak at 135 V, which may exceed the design limits. For example, if the nominal bus voltage is 400 V, and the design rules mandate that peak voltages are  $\leq 80\%$  of the rated voltage, then the 535 V peak voltage exceeds the limit even for a 650 V rated transistor. This suggests that the solution for using TO-247 packages and keeping overshoot voltage below 480 V is to slow-down the switching, by increasing the turn-on and turn-off gate-drive impedances, for example. Slowing down switching will of course also increase switching loss—which takes away from the benefit of using GaN transistors in the first place.

The surface-mount TOLL with single-sided return-path is the next-best option for low power-loop inductance. It's layout inductance with 9 A/ns applied would result in an 81 V overshoot—just at the design goal of 480 V peak assuming a 400 V bus. By adding the parallel return-path on the gate-side (the TOLL dual return-path), the loop inductance is now low enough that the overshoot voltage is 54 V, providing some additional margin so that even if the bus is pumped-up to 420 V, the added 54 V overshoot will stay below the 480 V design goal. All three of the bottom layouts in [Figure 11](#) have sufficiently low loop inductance, providing suitable options for either top-or bottom-side cooled packages.

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications

## Practical guidelines to get the best operation of HV and MV CoolGaN™

### Considerations for gate driver layout

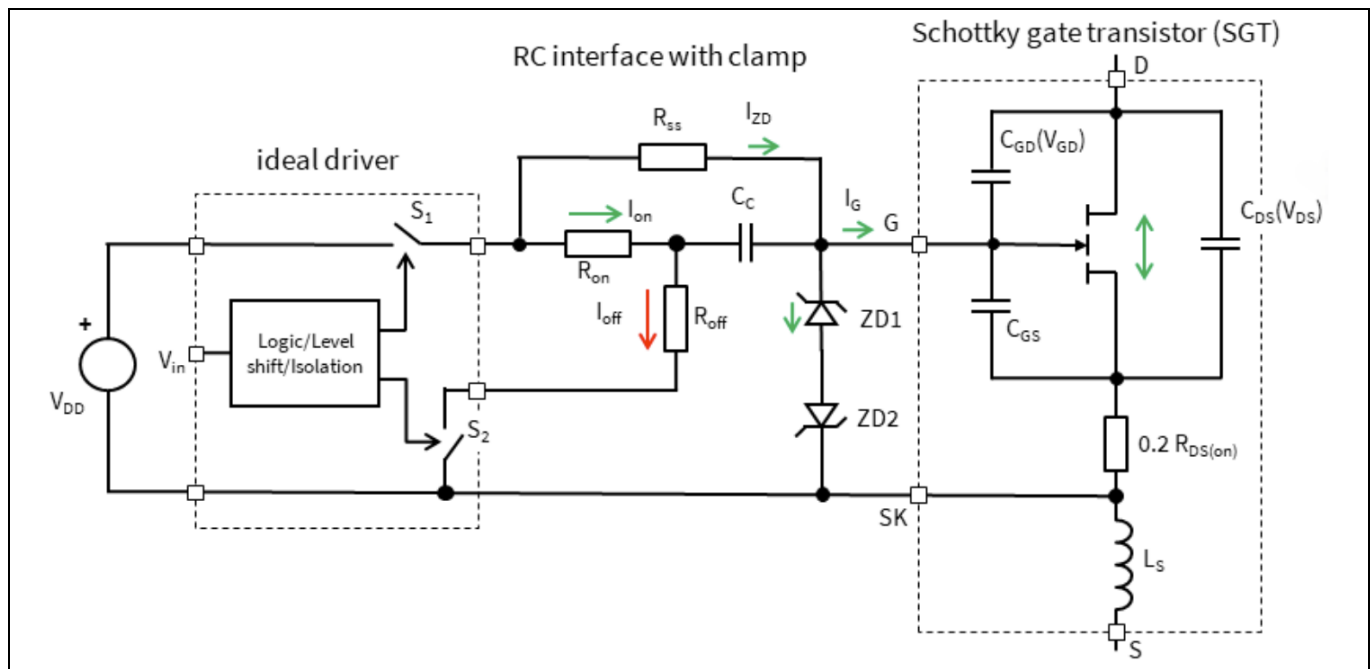
## 8 Considerations for gate driver layout

GaN transistors have low threshold voltages, typically in the range of 1–2 V. In addition, the fully-ON  $V_{GS}$  is in the range of 3.5–5 V, depending on the gate technology. Also, the transconductance of the transistor, as well as its gain-bandwidth, are quite high in the active region. This set of characteristics makes it imperative that the gate-drive loop must be low-impedance, otherwise the  $\frac{C_{GD}dV_{DS}}{dt}$  current injected through the “Miller” capacitance ( $C_{GD}$ ) will influence the gate voltage, resulting in ringing, overshoot, potentially high-frequency oscillation, and spurious turn-on leading to destructive cross-conduction or “shoot-through.”

One of the biggest challenges is keeping the gate off when a fast-rising  $dV/dt$  appears on its drain voltage. It is all but impossible to make the gate driver turn-off loop low-enough impedance when using separately packaged transistor and driver. This is primarily why negative gate-bias is used in discrete designs: to provide sufficient margin so that gate bounce voltage does not exceed the threshold during switching transients.

### 8.1 Gate driver circuit variants for Schottky-gate and GIT GaN transistors

Infineon uses two different gate structures in its CoolGaN™ transistors. Some of the high-voltage product line and all of the medium-voltage products use a Schottky-Gate. The other high-voltage GaN transistor uses an Ohmic gate contact, commonly called a Gate Injection Transistor or GIT. The term “injection” refers to hole injection, which occurs at both the gate p-GaN interface, as well as the Hybrid Drain p-GaN interface. The purpose of the hole injection is to manage trapped electrons and thereby reduce “dynamic  $R_{DS(on)}$ ” to insignificant levels.



**Figure 12** Example gate-drive layout with return-plane directly below the drive circuit

The Schottky-gate GaN transistors are driven similarly to logic-threshold Silicon MOSFETs, whereas the GIT has an intrinsic clamp-diode across the gate, which self-limits the gate voltage. The GIT is driven with a drive-circuit that emulates a current-source (commonly referred to as an RC network) from a standard gate-driver. Sometimes, the circuit designer wants to have the option to drive either the Schottky-Gate or the GIT (for second-source capability for example). This can be easily accomplished by adding two Zener-diodes to the

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standard GIT gate drive circuit as shown in [Figure 12](#). This circuit arrangement is called the EZDrive circuit. For more specific detail on proper design of any of these GaN gate-driver circuits, refer to the application note “Gate drive configurations for GaN power transistors” [2].

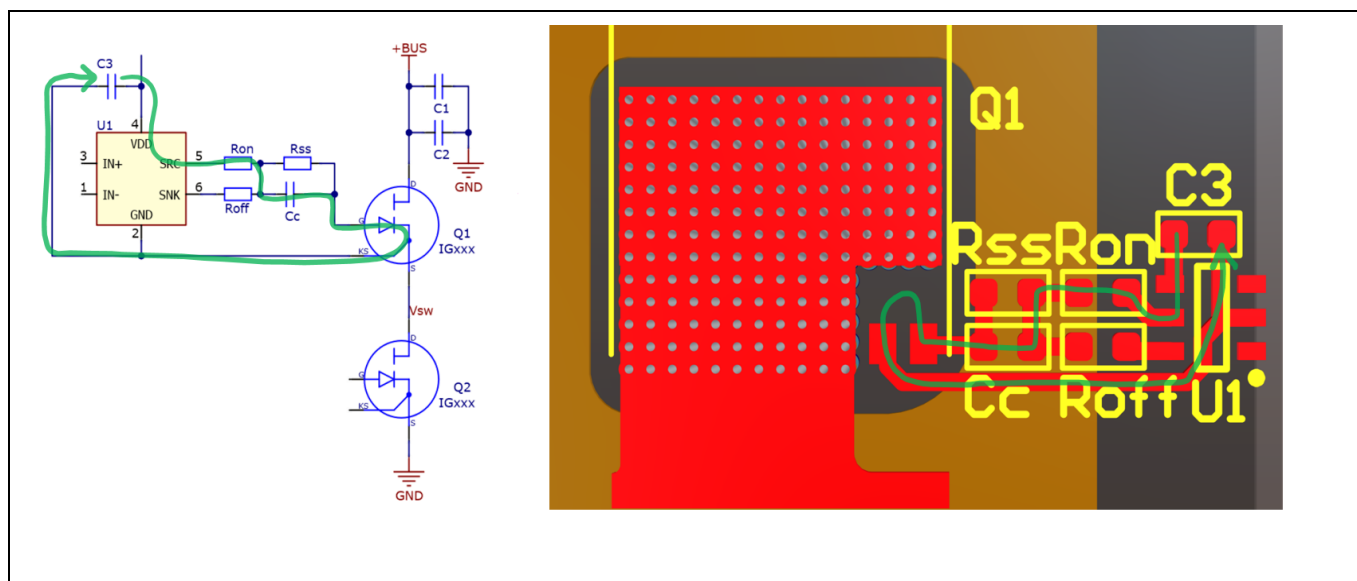
Regardless of the exact configuration of the circuit – whether it is a simple  $R_{ON}$  and  $R_{OFF}$  for a Schottky-gate, an RC network for the GIT, or the EZDrive circuit, the same concepts and recommendations apply for optimal PCB layout for these gate-driver circuits.

## 8.2 The two key concepts for optimum gate-driver layout

Since GaN transistors are capable of very fast switching speeds, in the single-digit ns range, the effective bandwidth of the voltage signals and transient currents in the gate driver circuit extend into the several hundred MHz frequency-range. This is why even small inductances in the gate drive loop can make a big difference. For example, a mere 1 nH in the gate-drive loop can result in 1.9  $\Omega$  of inductive reactance at an equivalent bandwidth of 300 MHz. Consequently, you can imagine that a few nH extra could completely dominate the  $R_{ON}$  or  $R_{OFF}$  resistor values, making the overall loop an underdamped RLC circuit, increasing the ringing and overshoot on the gate voltage.

**Key concept #1:** Place all of the gate-driver components over a return-common plane for minimum loop inductance.

This is the same concept discussed earlier as a method to reduce commutation-loop inductance: eliminate the lateral-loop and use only a vertical-loop. As an example, consider the circuit and layout in [Figure 13](#). The gate driver circuit for high-side Q1, along with the current-flow path for the current during turn-on is shown. In this example, all of the routing is on the top layer (red) of the PCB, because the next layer down (brown) is used for commutation loop. Note in particular that the return-path from Kelvin source back to U1 is as close as it can be on the top-layer and still meet the necessary spacing distances. The same circuit and layout is shown again in [Figure 14](#), but now it is the turn-off gate-drive current-loop that is highlighted with the green arrow. Once again, there is really no way to make the loop significantly smaller with everything routed on the top layer.

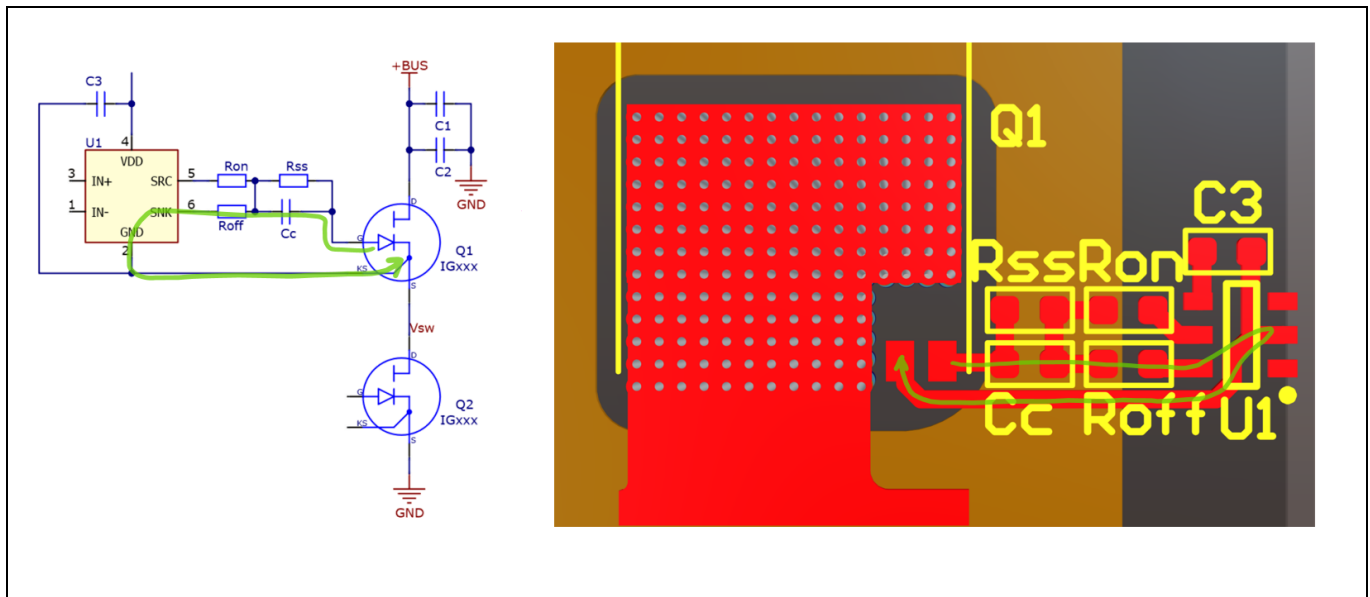


**Figure 13** Current path in a gate-driver lateral turn-on loop

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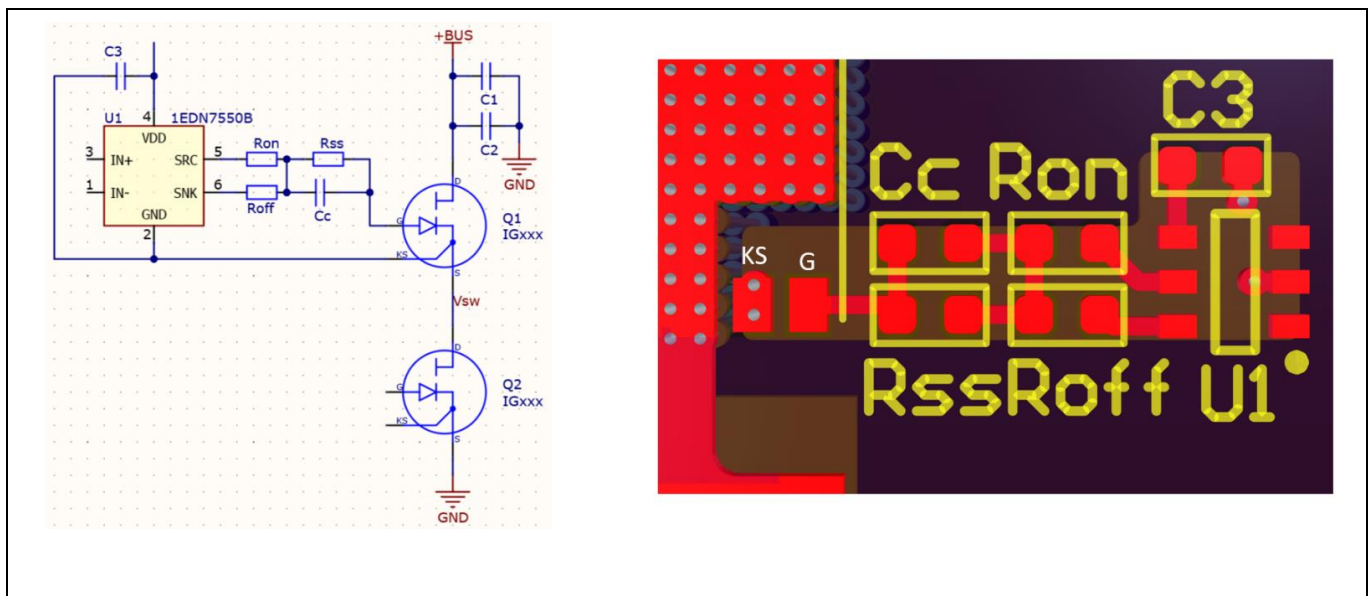
### Considerations for gate driver layout



**Figure 14** Current path in a gate-driver lateral turn-off loop

It seems to be a good layout – everything is in close-proximity to the transistor, all the paths are short and direct, and the return path is as close as possible on the same layer.

But is there a better way? Could this be significantly improved? The answer is yes. Look at the approximate loop dimensions in Figure 14. The turn-on loop is approximately 2.7 x 9.8 mm, as shown. The estimated loop inductance is about 12 nH. To further improve this layout, use layer-2 for the return-path instead.



**Figure 15** Same gate-driver circuit with return-path moved to layer-2 lowers loop inductance 5x

The improved layout is shown in Figure 15. Nothing has changed on the top layer, except for the return-path. Now, there is a copper polygon on layer-2, directly under the entire gate-driver circuit. This polygon is the new return-path. It is connected through vias to the top layer, at the Kelvin source of the transistor, and to the gate-driver ground at the connection between C3 and U1 ground. Why is this better than the lateral loop on the top layer? Just like in the previous examples of commutation loop optimization, the vertical loop is MUCH smaller

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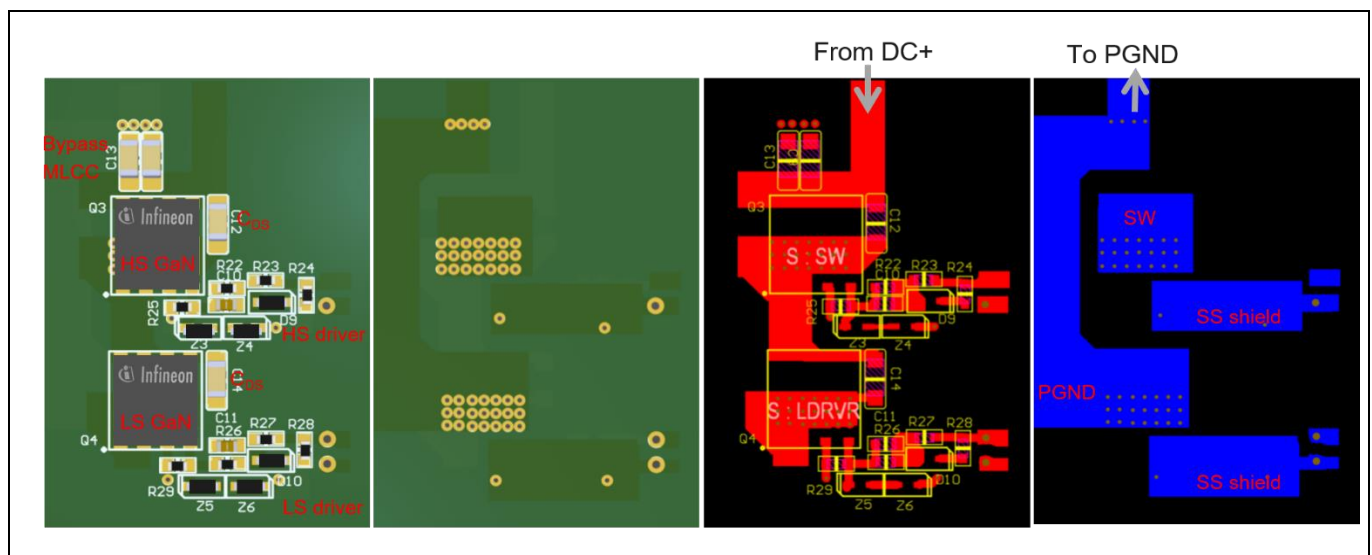
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than the lateral loop because the spacing between layers 1 and 2 is 0.18 mm in this example. Referring again to [Figure 15](#), the X-dimensions are the same, 9.8 mm. But, the previous Y-dimension of 2.7 mm is now replaced by a new Z-dimension of only 0.18 mm in the vertical loop, resulting in an estimated inductance of 2.5 nH – nearly a 5x improvement.

But – in order to realize this improved gate-driver circuit layout – the previous commutation-loop ground return-path must be eliminated in this area. That would mean either using the single-sided return-path configuration shown in [Figure 7](#) or perhaps using one of the top-side cooled packages.

Another example of this layout technique is shown in [Figure 16](#). In this example, a smaller DFN package is shown, along with the EZDrive gate circuit mentioned previously. On the left you can see the high and low-side transistors and gate circuits, and the right side shows the top-layer PCB in red, and the second layer in blue. The PGND return-path in the blue layer is exactly like the single-sided return shown in [Figure 7](#), and the gate circuits are placed on top of a gate-drive loop return plane (and shield) in layer-2, just like shown in [Figure 15](#).



**Figure 16** An example showing proper layout of the EZDrive gate circuit on a half-bridge using DFN packages

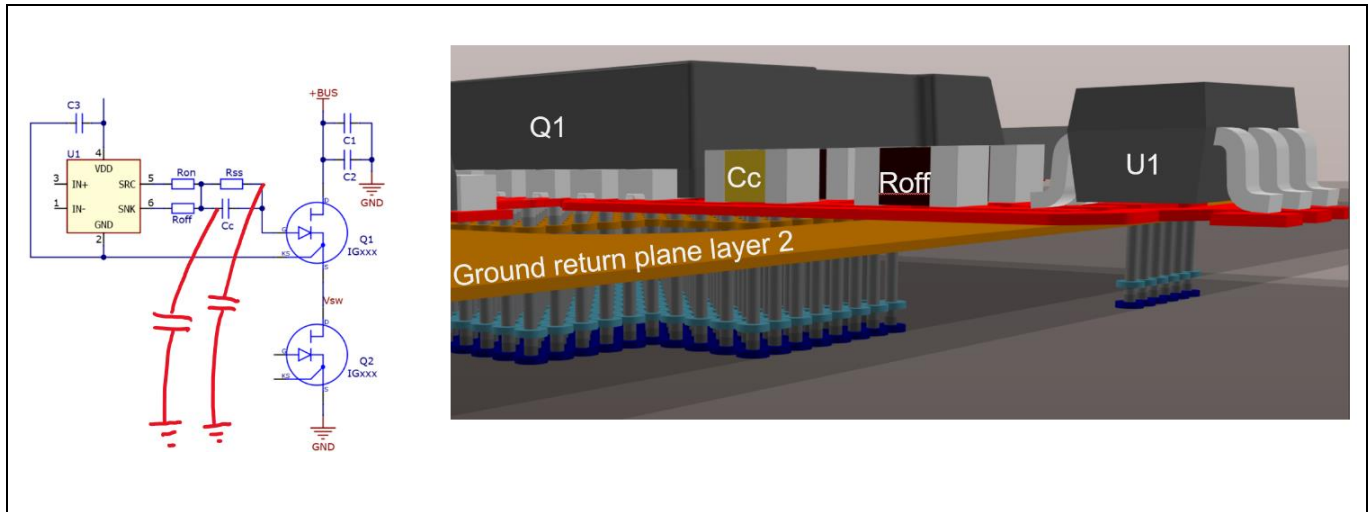
**Key concept #2:** The return-plane will also shield the gate circuit from disruptive capacitively-coupled currents, especially from the high-side to bus or ground-planes.

If you go back and look at [Figure 13](#) and [Figure 14](#), you may notice a second problem with the layout: The brown layer is the ground return for the commutation-loop (it is the same commutation return-arrangement as shown in [Figure 8](#)). This problem is much more challenging because the high-side gate driver circuit is located right on top of the ground plane for the DC bus. Even though the capacitance may be relatively small, the  $\Delta V$  is large – the full bus voltage. Moreover, the  $dv/dt$  across this capacitance is the same as the fast  $dv/dt$  of the switch-node. The simplified parasitic PCB capacitance is drawn in red on the schematic in [Figure 17](#). This type of layout will very likely experience problems due to the charge injected into the gate driver circuit on every switching edge.

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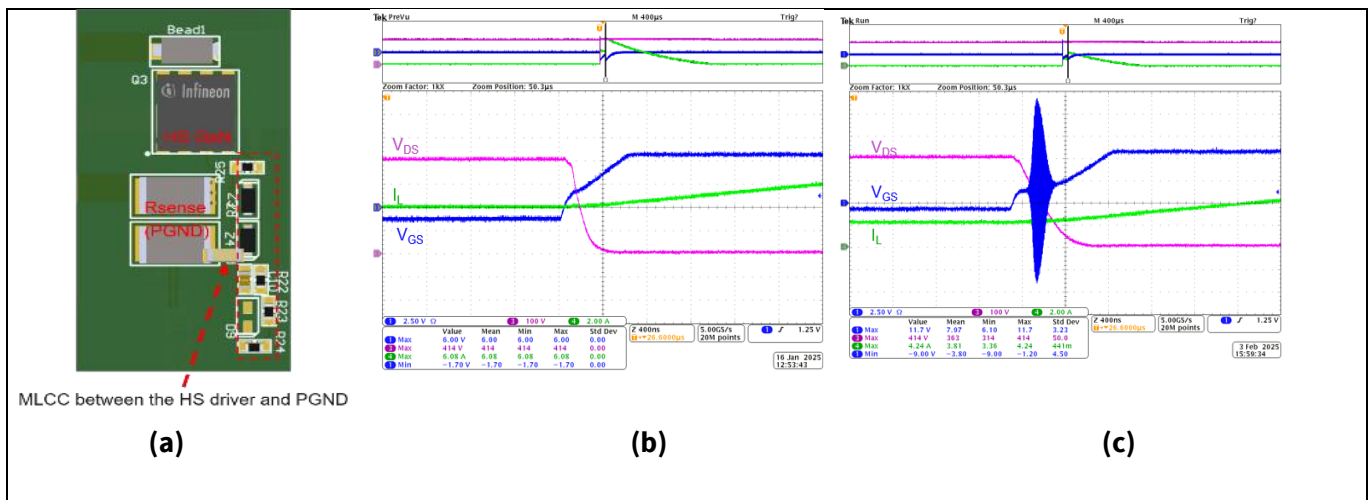
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**Figure 17** Problematic capacitance from high-side gate-driver circuit to ground

To illustrate the capacitance to ground effect, a 10 pF capacitor was placed between the high-side gate and ground nodes on a half-bridge circuit shown in Figure 18a. The normal turn-on of this half-bridge during a double-pulse test is shown in Figure 18b. Even though the turn-on  $dv/dt$  has been slowed down to 2 V/ns in this experiment, the 10 pF capacitance *further* slows the turn-on, and creates instability and oscillation seen in Figure 18c. Clearly, the high-side gate is susceptible to parasitic capacitance to ground.



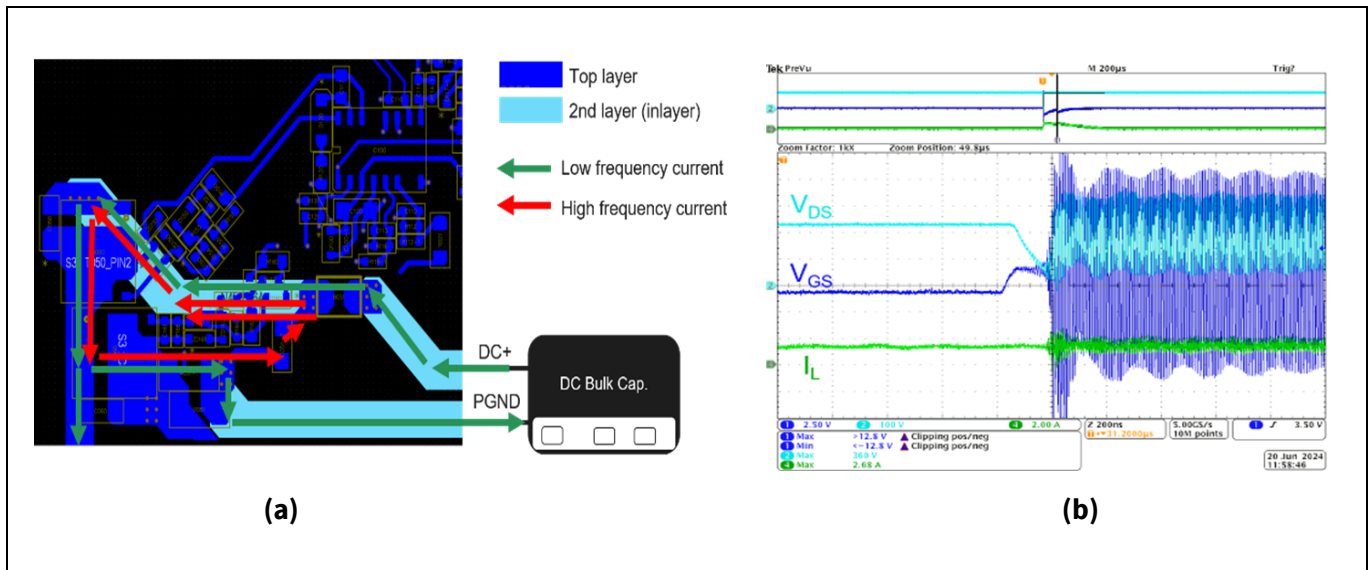
**Figure 18** Effect on turn-on waveform of capacitance added between high-side gate and ground

Another example is shown in Figure 19, where there are two combined effects impacting the gate-drive circuit, causing not only instability, but also sustained oscillation. The first effect is just like in the previous example, where the high-side gate drive circuit on the top layer crosses over the DC bus on the second layer. It doesn't matter whether the positive or negative side of the bus – both behave just like an AC ground. Thus, there is capacitance from the gate drive circuit to ground. But in addition, the commutation loop is a lateral loop, as indicated by the red arrows. This lateral loop injects an H-field into the gate-driver circuit as well. During commutation transients, the H-field transient induces emf into the gate driver loop. You can see the result in Figure 19b, where the hard-switched turn-on results in sustained oscillation.

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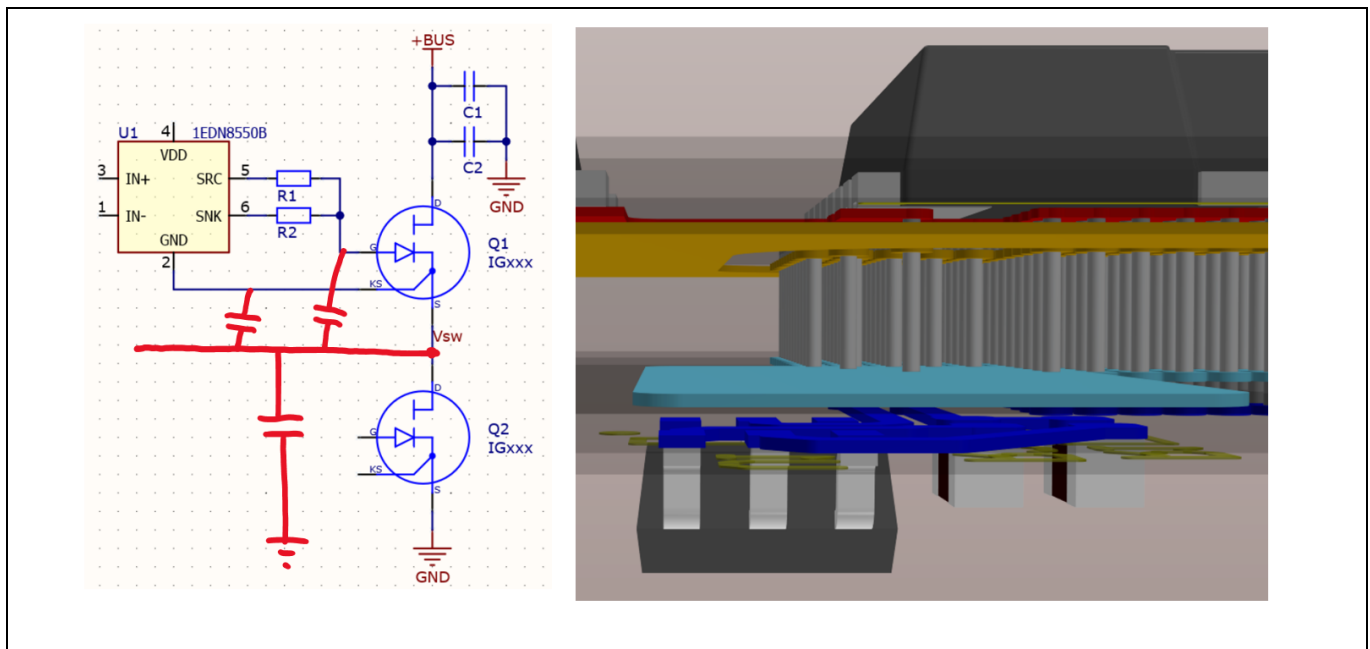
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**Figure 19** Example of oscillation caused by high-side gate-driver circuit crossing-over ground plane

This is an example of one of the compromises or tradeoffs that often must be made during a PCB layout: optimizing the gate driver layout results in a less-optimal power loop. Conversely, optimizing the power loop produces gate driver layout problems. Another approach to consider for the gate driver layout is to keep the double-sided return path for the power loop and move the gate driver circuit to the backside of the PCB. The gate driver loop then needs vias to connect to the transistor. Side-by-side vias provide a reasonably low impedance. This is shown in [Figure 20](#).



**Figure 20** Gate driver circuit on opposite side of PCB, with gate-driver return acting as driven Faraday shield

The layout of the gate driver is essentially the same, but it is relocated to the backside of the PCB and connected to G and S through vias. In this 4-layer example, the middle “core” of the PCB is much thicker than the spacing between layers 1-2 or 3-4. Thus, layer 2-3 has larger spacing and reduced capacitance. The

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capacitance to bus ground does not go away, but it is now between two low-impedance planes rather than coupling to the gate driver circuit and its components. Thus, the gate driver circuit only “sees” capacitance to its own local common, not to the bus ground plane. The current necessary to charge and discharge the inter-plane capacitance therefore comes directly from the low-impedance switch-node, completely bypassing the gate driver circuit.

Note that, regardless of the exact configuration of the gate drive circuit – whether it is just 2 R, or RC, or EZDrive – all of the principles discussed in this section apply equally.

## 9 General recommendations for MV GaN in synchronous rectification (SR)

Parallel connection of GaN switches with a good current sharing depends on both device and system level parameters, some of which are given below (see [Table 1](#)). Here, it can be observed that there are system and device level parameters, which affect the static and dynamic performance in paralleling. For instance, a switch technology with a positive temperature coefficient helps in static current sharing, where parameters such as gate threshold and transconductance have an impact in dynamic current sharing performance. Variations of these two parameters, due to mass manufacturing, comes on top of the temperature dependency as an additional challenge. Here, the designer has more control on factors such as PCB layout design, gate driver selection, and thermals.

**Table 1 Design parameters for paralleling power MOSFETs**

Design parameters	Effect on paralleling	Desired
$R_{DS(on)}$	Affect static current sharing	Positive temperature co-efficient for self-balancing
Gate threshold, $V_{GS(th)}$	Impact dynamic current sharing during turn-on and off. Lower $V_{th}$ results in earlier turn-on and higher switching current/loss which creates positive feedback	Tight distribution, temperature independent or positive temperature coefficient
Transconductance, gm	Impact dynamic current sharing during turn-on and off	Tight distribution, temperature independent or negative temperature coefficient
Circuit design and layout	Balanced circuit layout is important for dynamic current sharing and stability of the paralleling operation. This is particularly critical for high-speed power switches such as GaN/SiC	Minimize and equalize all layout parasitics to reduce circuit mismatch
Thermal	Affect the device temperature difference. $T_j$ variation may cause dynamic or static current sharing issues depending on device characteristics	All paralleled devices should have similar thermal resistance and installed on same heatsink for good thermal balance

GaN E-HEMTs exhibit a positive temperature coefficient for  $R_{DS(on)}$ , meaning their on-resistance increases with temperature. This strong temperature dependency is advantageous for parallel operation, facilitating current sharing among multiple devices. Simultaneously, GaN E-HEMTs also maintain a stable gate threshold voltage ( $V_{GS(th)}$ ) across a wide temperature range. This reduces dynamic current sharing difficulties in case of different junction temperatures of paralleled switches. Importantly, the transconductance (gm) of GaN E-HEMTs decreases with increasing temperature. This characteristic, combined with the stable  $V_{GS(th)}$ , contributes to dynamic current sharing and self-balancing in parallel configurations. This self-balancing effect is achieved through a negative feedback mechanism: as junction temperature ( $T_j$ ) rises, gm decreases, leading to a reduction in drain current ( $I_D$ ) during switching and consequently a lower on-state energy loss ( $E_{on}$ ), lowering  $T_j$ . This inherent self-regulation promotes stable and efficient parallel operation of GaN E-HEMTs.

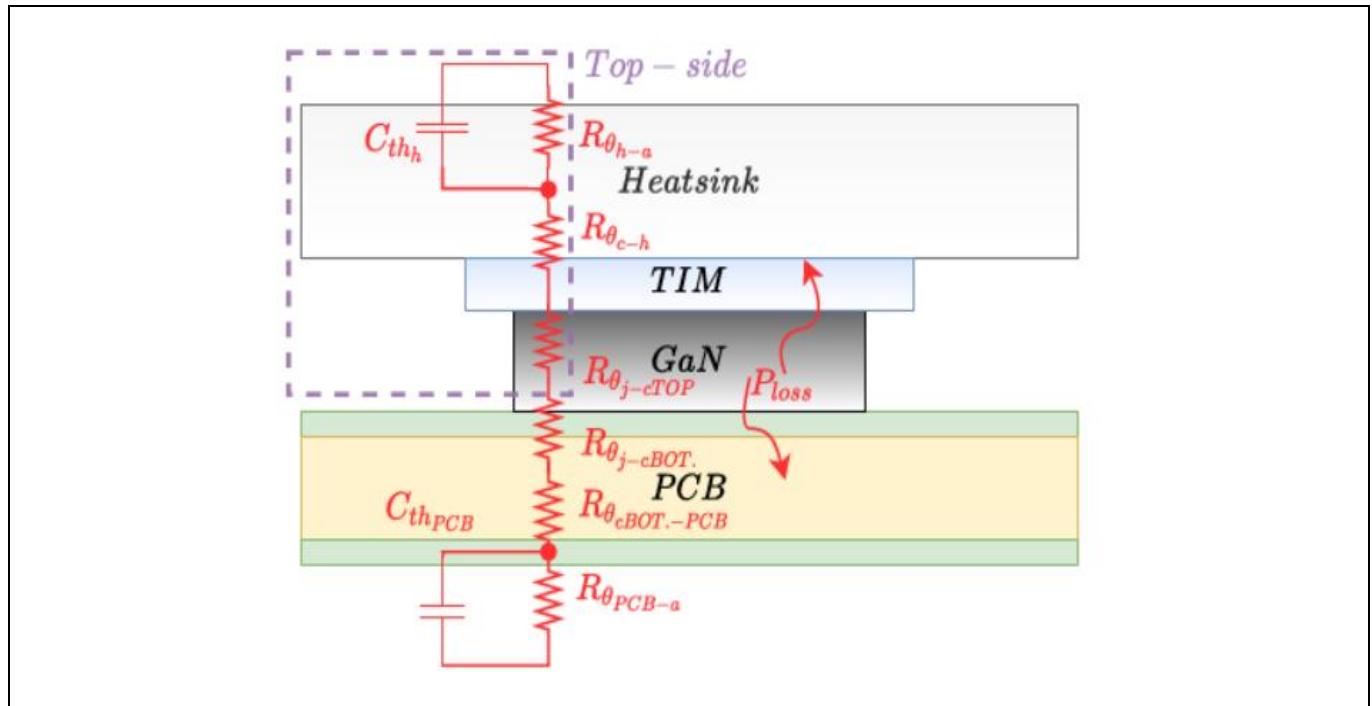
Cooling strategy is crucial in proper paralleling of synchronous rectifier switches. In high-power SMPS secondary layouts, due to the high density of the components and high currents, extraction of heat becomes a

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challenge. It is possible to use multiple PCB layers for heat transfer and thermal vias for reducing the case to ambient thermal resistance. In addition, top-side cooling can be used as an effective method of heat spreading thanks to CoolGaN™ packages with dual side cooling feature. Figure 21 shows the cross section of a GaN cooling configuration], where thermal resistances of junction-to-case(top), case(top)-to-heatsink (thermal interface material, TIM), and heatsink-to-ambient has been shown for the top side cooling of the switch in addition to the thermal resistances of junction-to-case(bottom), case(bottom)-to-PCB, and PCB-to-ambient.



**Figure 21 Thermal cross section of a GaN switch with top and bottom-side cooling options**

Bottom-side cooling of CoolGaN™ transistors is possible through thermal vias. This way, it is possible to spread the heat to other PCB layers, especially to the opposite side of the PCB, where a heatsink is mounted. PCB copper thickness plays a key role here for better heat transfer throughout the layers. While staggering the vias between adjacent pads can help to increase the distance between them, it is also crucial to consider the thermal connection to the switch-node path, as this is the only thermal/electrical net shared by both transistors in the half-bridge configuration. The switch-node can sometimes be extremely hot due to the transformer connected there. In such cases, it is not advantageous to thermally couple this heat to the transistors. However, the transformer can sometimes function as a heatsink due to its high surface area if its operating temperature is not remarkably high.

Due to the reduced  $R_{ds(on)}/Area$  values of GaN transistors, it is possible to have smaller packages for the same on-resistance values compared to Si switches. In order to compensate the reduced cooling capability, top-side cooling might need to be used. The recommendations for GaN dual-side cooling are similar to those for MOSFETs, as explained in [2]. GaN-specific recommendations are further explained in [3] and [4]. This section will offer a brief overview focusing on one design example, while these references provide deeper insights on top-side and dual-side cooling techniques.

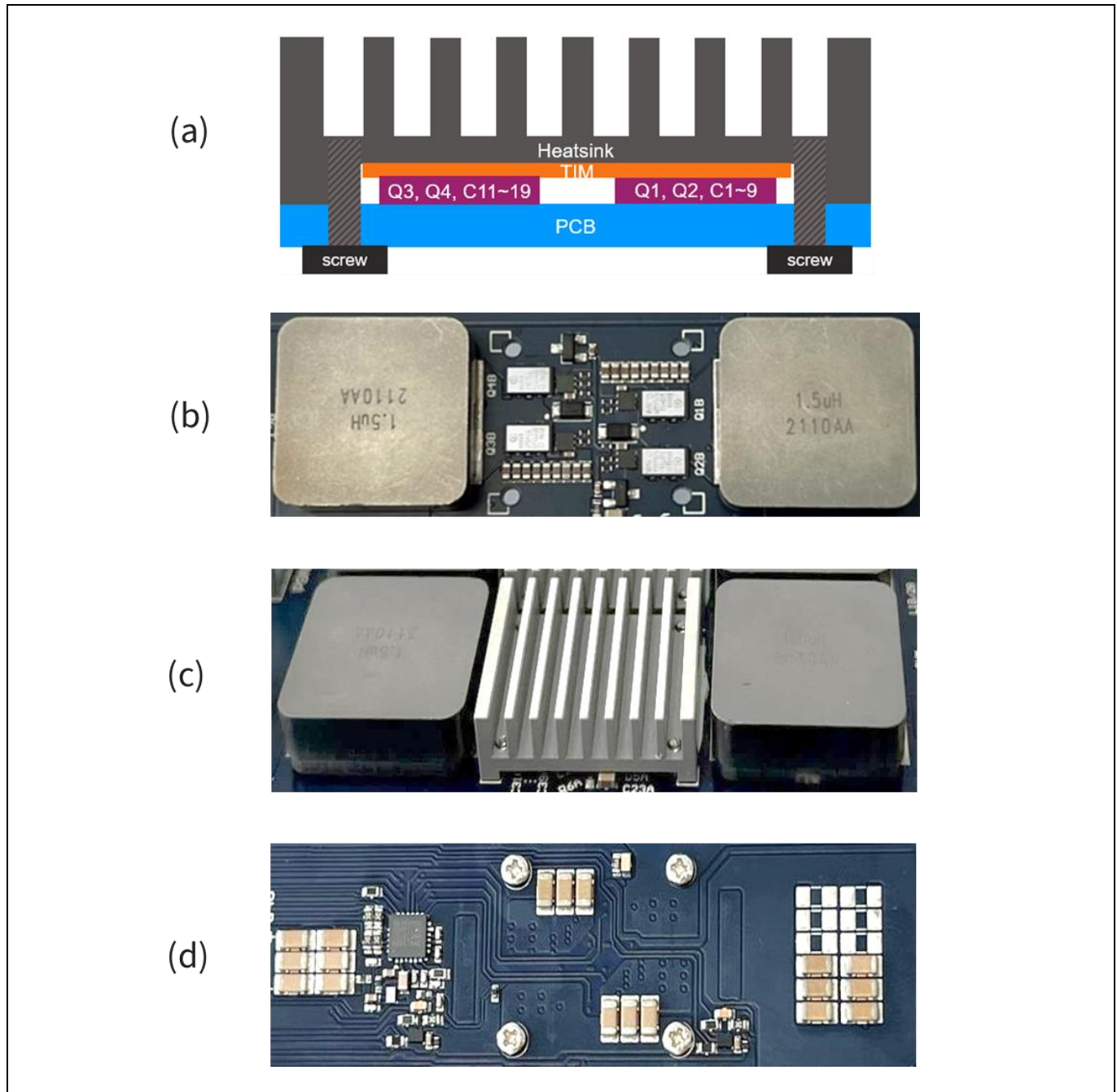
Figure 22 demonstrates the thermal design implemented in an example multi-phase buck converter design [5]. The heatsink is mounted with a fixed gap, rather than a fixed pressure. Fixed-gap assemblies use a shim, projection, or rail on the heatsink to define the distance between the PCB and the underside of the heatsink. The gap between the heatsink and CoolGaN™ transistor is that distance minus the transistor's seated height (package

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height + solder paste). In the example shown below, the heatsink stands off from the PCB at a height of 1.2 mm. The seated height of the CoolGaN™ transistor is approximately 1.0 mm<sub>max</sub>. These leaves ~0.2 mm to be filled by a compressed thermal interface material (TIM). This design uses an ultra-soft pad TGA-1780 with 0.5 mm uncompressed thickness, allowing for some tolerance in the dimensions without leaving an air gap.



**Figure 22** Example top-side cooling design with fixed-gap approach (a) Simplified diagram, (b) Top view before heatsink is installed, (c) Top view after heatsink is installed, (d) Bottom view after heatsink screws are installed

Many options are available for the TIM, either as a pad or as a curable liquid/paste, with thermal conductivities in the range of 4~18 W/m-K. The top-side cooling pad area is specified in the MV CoolGaN™ datasheet, and the thermal resistance of the TIM can usually be calculated using temperature curves or values in its own datasheet.



## **Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications**

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### **Practical guidelines to get the best operation of HV and MV CoolGaN™**

#### **General recommendations for MV GaN in synchronous rectification (SR)**

As far as the gate loop, to optimize performance, position the driver and its associated device on the same layer, minimizing the distance between them and the power supply capacitor. Critically, locate the driver current's return path on the layer immediately below the components, again minimizing the distance between the component layer and the return path layer for optimal signal integrity and reduced noise. In addition to gate loop, power loop also required careful design. For optimal performance, place all devices and input filtering capacitors on the same layer. Minimize the distance between the input capacitors and ground (GND). Route the return path for the power current on the layer directly below the component layer, keeping the distance between these layers as short as possible.

## 10 Summary: Key recommendations for optimizing performance of high-speed HV GaN transistors

The table below provides a summary of the key points discussed in this article.

**Table 2 Recommendations and further considerations for optimizing performance of high-speed HV GaN transistors**

Recommendation	Further considerations
Consider where current will flow during switching transitions	Be sure to include parasitic elements in that assessment. Remember to include the complete return-path of the current in the analysis.
Layout inductance may be critical in some parts of the circuit, but unimportant in others	Recall the “half-bridge as a two-port network” in Section 3
Minimize layout inductance by taking advantage of PCB layer pairs with thin dielectric	Route outbound and return currents along the same path, but on adjacent parallel layers in opposite directions
Avoid deviations from the “over/under same path” that will result in lateral loops	As well as lower mutual inductance and therefore higher loop inductance
Remember: package inductance is not necessarily a fixed value for any SMT package	The value should be dependent on the assumed return path
Use top-side cooled SMT packages to optimize both the electrical and thermal paths, independently	Without having to make compromises or increase cost from adding more than 100 thermal vias
Use a plate for the return-path of gate driver circuits	Directly below the circuit, connected to the KS pin
Prevent capacitive currents	From switch-node to ground from flowing through KS pin
Keep ground reference circuits away from high-side gate driver circuit	Or use a driven Faraday shield if that is not possible
Keep the switch-node compact	To minimize capacitance and radiation into other parts of the circuit
Keep HS driver away from PGND	Maintain a safe distance between the HS driver and the PGND to prevent noise coupling and interference
Avoid High-Frequency Current cross-over the driver circuit	Keep high-frequency currents away as far as possible from the drive circuit to prevent noise coupling
Prevent HS/LS GaN Overlap	Ensure that the HS and LS GaN devices do not overlap to prevent noise coupling and interference

The fast-switching capability of GaN transistors can make PCB layout more challenging. This article discussed several key concepts to help the user understand the layout challenges, and strategies to help solve these challenges and optimize the layout for best overall electrical and thermal performance.

Following the recommendations explained in this document and summarized in the table above will help designers obtain optimal performance from high-performance GaN technology.

## 11 Related resources

- [GaN transistors \(GaN HEMTs\)](#)
- [E-mode and D-mode GaN power transistors: real-world performance compared to theory](#)
- [Gallium nitride - Reliability and qualification of CoolGaN™ GIT HEMTs](#)
- [Gate drive configurations for GaN power transistors](#)
- [2500 W full-bridge totem-pole power factor correction using CoolGaN™](#)
- [An industry game-changer: 300 mm power GaN technology](#)

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- [1] Clayton, Paul: *Inductance: Loop and Partial*; Wiley; 2010; [Available online](#)
- [2] Bernhard Zojer, Infineon Technologies AG: *Gate drive configurations for GaN power transistors*; [Available online](#)
- [3] Bernhard Zojer, Francesco Di Domenico, and Eric Persson, Infineon Technologies AG: *Operation and features of high-voltage CoolGaN™ Transistor*; [Available online](#)
- [4] Persson, Eric: *PCB Layout Techniques for Optimizing Performance of Surface-Mounted Wide-Bandgap Power Electronic Circuits*; IEEE APEC 2022; Professional Education Seminar in 2022 IEEE Applied Power Electronics Conference and Exposition (APEC). 2022
- [5] Persson, Eric: *Optimizing PCB layout for HV GaN power transistors*; IEEE Power Electronics Magazine 10.2 (2023): 5-78; [Available online](#)

# Optimizing PCB layout for CoolGaN™ power transistors in SMPS applications



Practical guidelines to get the best operation of HV and MV CoolGaN™

## Revision history

### Revision history

Document revision	Date	Description of changes
V 1.0	2023-07-28	Initial release
V 2.0	2025-09-11	<ul style="list-style-type: none"><li>• Updated to latest template</li><li>• Updated Section <a href="#">7</a>, <a href="#">8</a>, and <a href="#">9</a></li></ul>

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