# How to use GaN synchronous rectifier (SR) for higher power

## Tips and tricks in parallelling GaN SR

## About this document

### Scope and purpose

This document provides an overview of hardware design guidelines for switched-mode power supplies (SMPS) applications using gallium nitride (GaN) synchronous rectifier (SR) with stage paralleling architecture.

### Intended audience

The document is intended for design engineers to consider the while designing the GaN transistor with stage paralleling architecture.

### Keypoints

- Provides detailed hardware design guidelines for GaN-based synchronous rectifiers (SR) in SMPS, focusing on high-power and high-efficiency applications within compact spaces
- Provides practical insights into critical design aspects, such as current sharing, PCB layout, gate driver circuitry, and thermal management to optimize system performance
- Highlights the practical limits of GaN SR paralleling, enabling improved efficiency, effective thermal dissipation, and reliable performance in high-power SMPS designs

## About this product family

### Product family

Infineon's CoolGaN™ solution offers unmatched quality that operate at higher switching speeds resulting in lower power losses, higher efficiency paving the way for smaller and lighter power supplies with the same power supplies with the same size but increased power capability.

### Target applications

- Consumer electronics
- Information and Communication Technology
- Motor drives
- Robotics
- Energy Storage Systems
- Renewables

Please read the sections "Important notice" and "Warnings" at the end of this document

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# 1 Introduction

There is a continuous demand for higher power in limited spaces with higher efficiencies for switched-mode power supplies (SMPS), which brings the need for switch or stage paralleling depending on the preferred architecture. Synchronous rectifier (SR) switch power loss budget in SMPS is dominated by conduction losses that requires several low $R_{DS(on)}$/area SR switches connected in parallel for high power SMPS. In this case, topics such as current sharing, PCB layout, gate driver circuitry, and thermal management becomes critical.

In this document, the practical aspects of GaN-based SR design is discussed with emphasis on PCB layout. Practical limits of GaN SR paralleling are considered and performance metrics, such as efficiency and thermal management.

# 2 SR paralleling considerations

Parallel connection of GaN switches with a good current sharing depends on both device and system level parameters, a few are mentioned in Table 1. For more details, see [1]. Observe that there are system and device level parameters that affect static and dynamic performance in paralleling. For instance, a switch technology with a positive temperature coefficient helps in static current sharing, where parameters such as gate threshold and transconductance have an impact in dynamic current sharing performance. Variations of these two due to mass manufacturing comes on top of the temperature dependency as an additional challenge. Here, the designer has more control on factors, such as PCB layout design, gate driver selection, and thermals.

**Table 1** **SR paralleling considerations**

| Design parameters | Effect on paralleling | Required |
|---|---|---|
| $R_{DS(on)}$ | Affect static current sharing | Positive temperature co-efficient for self-balancing |
| Gate threshold, $V_{GS(th)}$ | Impact dynamic current sharing during turn-on and off. Lower Vth results in earlier turn-on and higher switching current/loss which creates positive feedback | Tight distribution, temperature independent, or positive temperature co-efficient |
| Transconductance, $g_m$ | Impact dynamic current sharing during turn-on and off | Tight distribution, temperature independent, or negative temperature co-efficient |
| Circuit design and layout | Balanced circuit layout is important for dynamic current sharing and stability of the paralleling operation. This is particularly critical for high-speed power switches such as GaN/silicon carbide (SiC) | Minimize and equalize all layout parasitics to reduce circuit mismatch |
| Thermal | Affect the device temperature difference. Tj variation can cause dynamic or static current sharing issues depending on device characteristics | All paralleled devices must have similar thermal resistance and installed on the same heatsink for good thermal balance |

GaN power transistor exhibit a positive temperature coefficient for $R_{DS(on)}$, where their on-resistance increases with temperature. This strong temperature dependency is advantageous for parallel operation, facilitating current sharing among multiple devices. Simultaneously, GaN power transistors maintain a stable gate threshold voltage ($V_{GS(th)}$) across a wide temperature range. This reduces dynamic current sharing difficulties in case of different junction temperatures of paralleled switches. Importantly, the transconductance ($g_m$) of GaN power transistor decreases with increasing temperature. This characteristic, combined with the stable $V_{GS(th)}$, contributes to dynamic current sharing and self-balancing in parallel configurations. This self-balancing effect is achieved through a negative feedback mechanism: as junction temperature ($T_J$) rises, $g_m$ decreases, leading to a reduction in drain current (ID) during switching and consequently a lower on-state energy loss (Eon), lowering $T_J$. This inherent self-regulation promotes stable and efficient parallel operation of GaN power transistors.

Cooling strategy is crucial in the proper paralleling of synchronous rectifier switches. In high-power SMPS secondary layouts, due to the high density of the components and high currents, extraction of heat becomes a challenge. It is possible to use multiple PCB layers for heat transfer and thermal vias for reducing the case to ambient thermal resistance.

Additionally, top-side cooling can be used as an effective method of heat spreading with the CoolGaN™ packages with dual-side cooling feature. Figure 1 shows the cross section of a GaN cooling configuration, where thermal resistances of junction-to-case (top), case (top)-to-heatsink (thermal interface material, TIM), and heatsink-to-ambient has been shown for the top-side cooling of the switch in addition to the thermal resistances of junction-to-case (bottom), case (bottom)-to-PCB, and PCB-to-ambient.

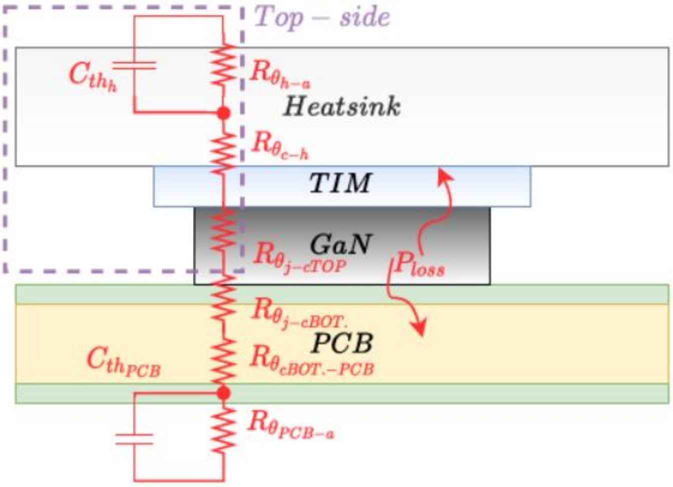


**Figure 1** **Thermal cross section of a GaN switch with top and bottom side cooling options**

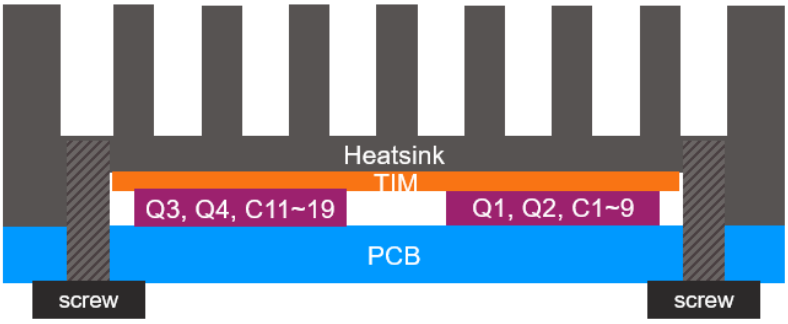
Bottom-side cooling of CoolGaN™ power transistors is possible through thermal vias. This way it is possible to spread the heat to other PCB layers, especially to the opposite side of the PCB, where a heatsink is mounted.

PCB copper thickness plays a key role for better heat transfer throughout the layers. It is also helpful to stagger the vias between adjacent pads to increase the distance between them. It is also important to consider the thermal connection to the switch-node path. This is the only thermal/electrical net shared by both transistors in the half-bridge. The switch-node can sometimes be extremely hot due to the transformer connected there, and then it is not advantageous to thermally couple this heat to the transistors. However, the transformer can sometimes function as a heatsink due to its high surface area if its operating temperature is not remarkably high.

Due to the reduced $R_{DS(on)}$/area values of GaN transistors, it is possible to have smaller packages for the same on resistance values compared to silicon (Si) switches. In order to compensate the reduced cooling capability, top-side cooling might need to be used. The recommendations for GaN dual-side cooling are similar to those for MOSFETs, as explained in [1]. GaN-specific recommendations are further explained in [3] and [4]. This section will provide a brief overview focusing on one design example, while these references provide deeper insights into top-side and dual-side cooling techniques.

Figure 2 demonstrates the thermal design implemented in an example multi-phase buck converter design [5]. The heatsink is mounted with a fixed gap, rather than a fixed pressure. Fixed-gap assemblies use a shim, projection, or rail on the heatsink to define the distance between the PCB and the underside of the heatsink. The gap between the heatsink and CoolGaN™ power transistor is that distance minus the transistor's seated height (package height + solder paste). In the example shown below, the heatsink stands off from the PCB at a height of 1.2 mm. The seated height of the CoolGaN™ power transistor is approximately 1.0 $mm_{max}$. This leaves ~0.2 mm to be filled by a compressed thermal interface material (TIM). This design uses an ultra-soft pad

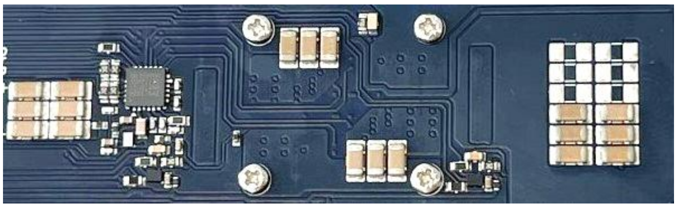
TGA-1780 with 0.5 mm uncompressed thickness, allowing for some tolerance in the dimensions without leaving an air gap.



(a) Simplified diagram

(b) Top view

(c) Top view after heatsink is installed



(d) Bottom view after heatsink screws are installed

**Figure 2** **Example of top-side cooling design with fixed-gap approach**

Many options are available for the TIM, either as a pad or as a curable liquid/paste with thermal conductivities in the range of 4~18 W/m-K. The top-side cooling pad area is specified in the CoolGaN™ bidirectional switch (BDS) datasheet and the thermal resistance of the TIM can usually be calculated using curves or values in its own datasheet. The choice of TIM is often a tradeoff between thermal performance and cost, as the highest conductivities sometimes come with the highest price tags.

# 3 Design considerations

Synchronous rectifiers (SRs) work with zero voltage turn-on (ZVT) as the primary current in an isolated converter is forced through the transformer to the secondary circuitry. This current discharges the $C_{oss}$ of the SR switches before their channels are on, preventing voltage-current overlaps in the drain-source channel and allowing a soft turn-on with ideally no losses. The rate of change of drain-source voltage ($V_{ds}$) during turn-on depends on the output capacitance of the switch, $C_{oss}$ and the leakage inductance of the transformer with respect to the secondary terminals. To conclude that the commutation mechanism during the SR turn-on is not similar to a hard switching half-bridge converter such as buck where there is voltage–current overlap during switching and loop inductance needs to be minimized to have faster turn on for lower switching losses. On the other hand, layout is still important since in full bridge SR configuration, turn-off voltage spikes still depend on power loop layout and loop inductance. In addition, SR gate loop inductance still plays a key role in gate oscillations and current sharing in parallel operation. Figure 3 shows a typical half-bridge configuration with gate driver circuitry using a half-bridge driver, where green and blue regions imply gate loop and power loop critical regions, respectively.

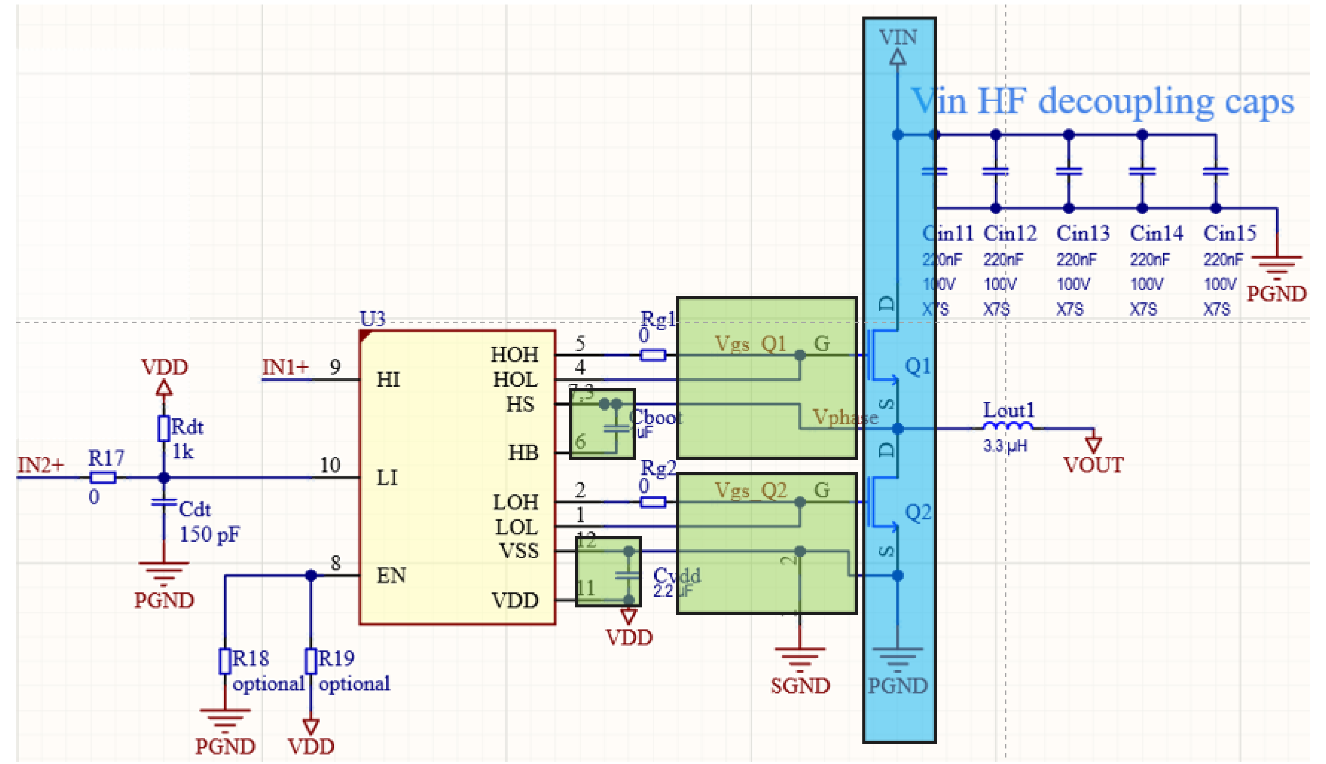


**Figure 3** Half-bridge with CoolGaN™ power transistor schematic with dual-channel driver

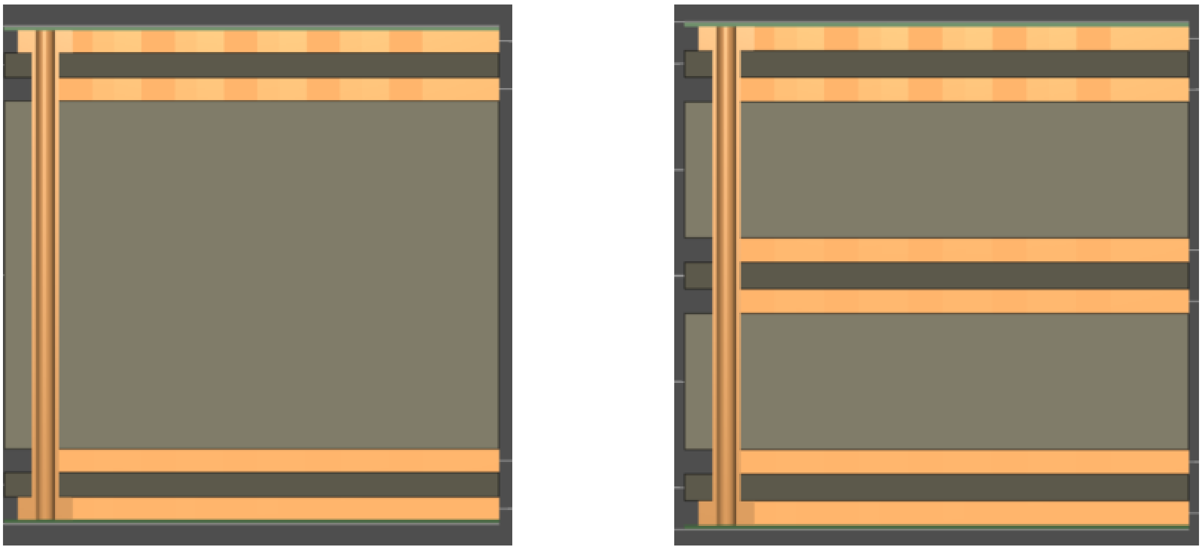
As far as the gate loops are concerned, optimize the performance by positioning the driver and its associated device on the same layer, minimizing the distance between them and the power supply capacitor. Critically, locate the driver current's return path on the layer immediately below the components, again minimizing the distance between the component layer and the return path layer for optimal signal integrity and reduced noise. For power loop, for optimal performance, place all devices and input filtering capacitors on the same layer. Minimize the distance between the input capacitors and ground (GND). Route the return path for the power current on the layer directly below the component layer, keeping the distance between these layers as short as possible.

## 3.1 PCB layer stackup

PCB stackups can generally be grouped into two categories: equal layer spacing throughout, and differential pairs. It can be difficult to manage the tradeoff between loop inductances and parallel plate capacitance in a PCB with equal spacing between all layers, so this is not the best choice in a GaN design. A differential pair stackup uses alternating thick and thin cores/prepregs, so that each layer is paired with exactly one closely spaced layer, while the gap to its other adjacent layer is much wider. A few examples are shown in Figure 4.

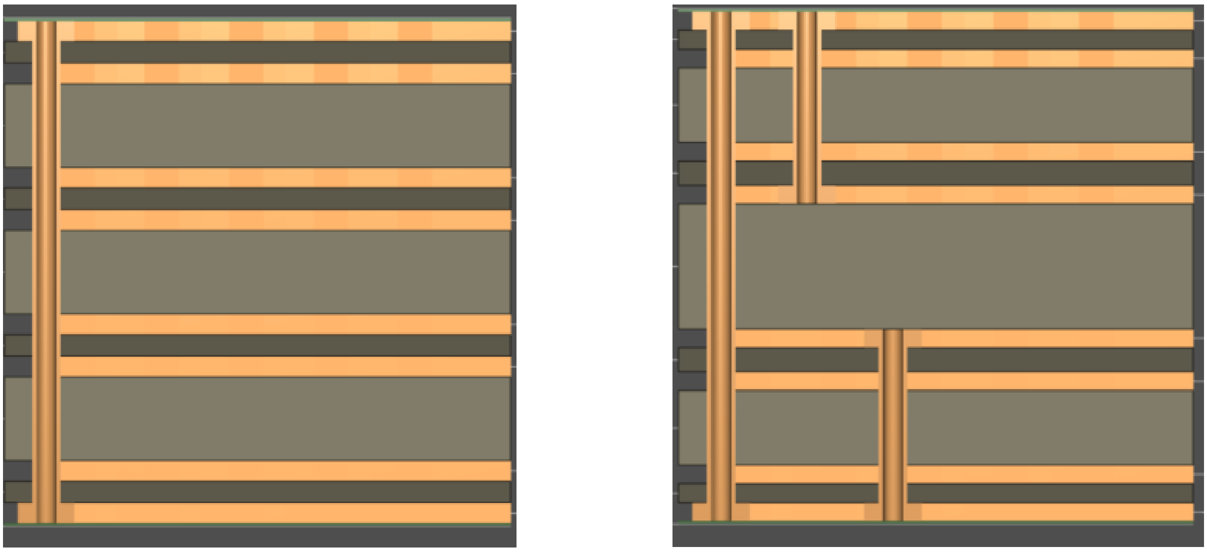
The simplest version of a differential pair stackup is the 4-layer PCB shown in Figure 4(a) with one thick core in the center and thinner prepregs beneath the outermost copper layers. This same approach can be applied with more layers, as shown in Figure 4(b) and Figure 4(c). In a system design with noisy switching circuits on one side (e.g., top layer) and sensitive control/communication circuits on the other side (e.g., bottom layer), it may be useful to apply a stackup as shown in Figure 4(d). Here, four layers can be designated for switching circuits while four layers are dedicated to control/communication and each half of the stackup has its own blind via type that can be used independently of the other half. The differential layers can be used for shielding or for extra parallel current-carrying copper. The thick dielectric on either side of the pair limits the parallel plate capacitance across that dielectric, providing more freedom to the designer in making these designations.

The dielectric thickness below the outermost two layers is usually the most critical. One or both sides of the board have power transistors and/or gate drivers, as well as the associated decoupling capacitors to define the switching loops. The outer layer has a close space first inner layer to close the loop and cancel the magnetic field directly below the outer layer copper. Depending on the copper thickness and manufacturing design rules, it may be possible to reduce this spacing to 50~120 µm. With an outer copper weight of 70 µm (2 oz.), a thickness of 80 µm is a good target.



(a) 4-layer stackup

(b) 6-layer stackup

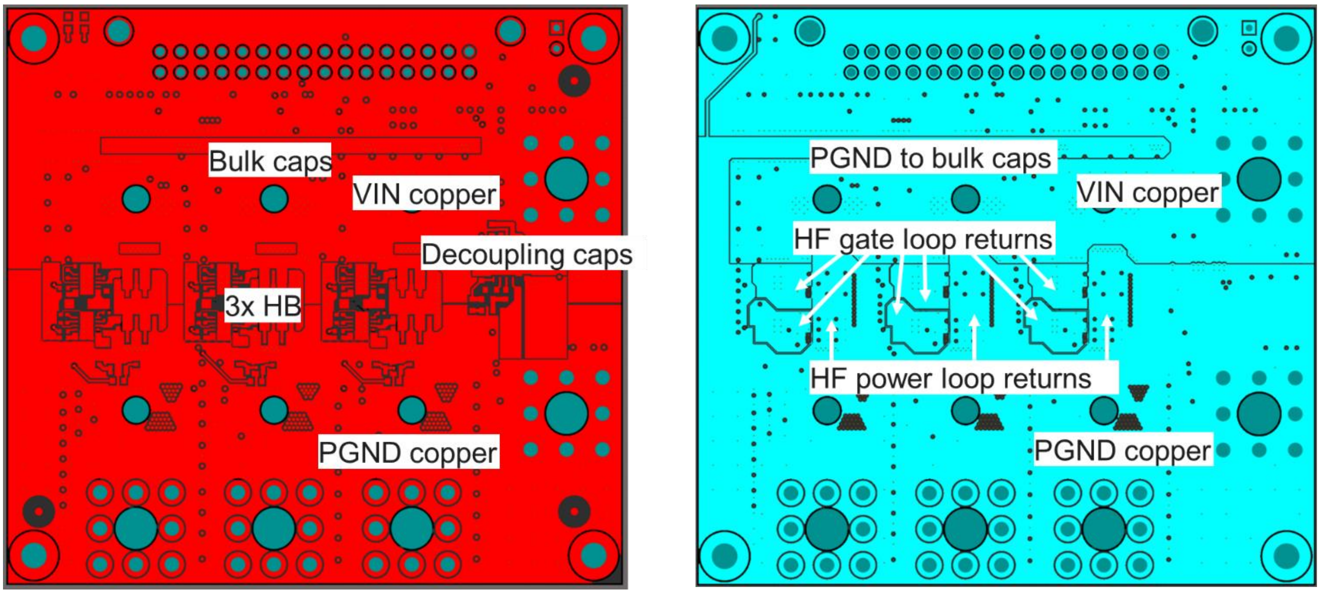


(c) 8-layer stackup with only through-hole vias (d) 8-layer stackup with through-hole and blind vias

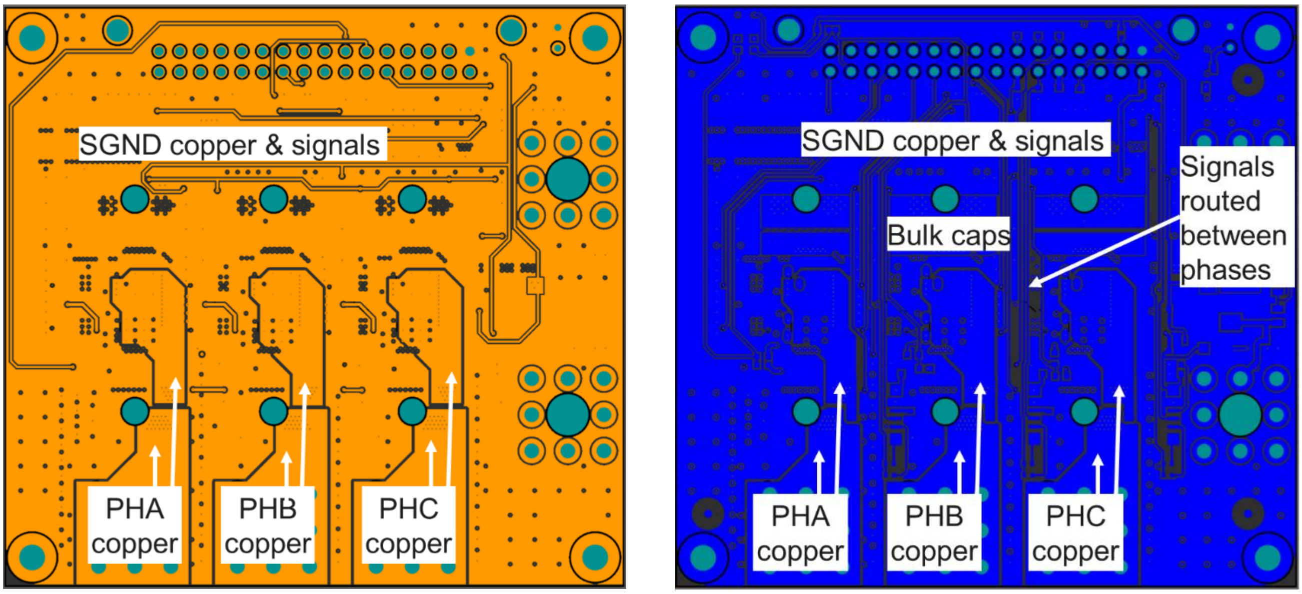
**Figure 4** **Example PCB stackups recommended for CoolGaN™ BDS designs**

## 3.2 Board area mapping

Positions of connectors (input power, output power, control/communication interfaces) as well as the half-bridges and other functional blocks of the system schematic affect performance. Mapping out these areas is an important step before the actual layout process begins. Poor mapping can result in parallel plate capacitance issues and signal coupling glitches. Figure 5 shows the four layers of a motor drive evaluation board as an example.



(a) Top copper layer (b) Mid-layer 1



(c) Mid-layer 2 (d) Bottom copper layer

**Figure 5** **Example PCB layer architecture for a motor drive design**

On the top layer, the three half-bridges are laid out as described in Section 3.3, including the CoolGaN™ power transistors, EiceDRIVER™ gate driver ICs, bootstrapping circuits, and decoupling capacitors. The remainder of this layer is reserved for DC power circuits, especially wide copper polygons for efficient flow of input power from the input supply voltage (VIN) and power ground (PGND) connectors. This also includes bulk capacitors to manage the voltage ripple. Because the switching frequency is multi orders of magnitude lower than the equivalent frequency of the switching commutation/transition, the inductance is not as critical here. However, it is important to minimize the resistance between power connectors and bulk capacitors, as well as between the bulk capacitors and the components within each half-bridge (decoupling capacitors and transistors). The first inner layer (mid-layer 1) contains the PGND shielding/return for the power loop, as well as copious PGND and VIN copper to further improve the flow of input power from the connectors to capacitors. The only exceptions are the shielding islands for each high-side gate loop.

The bottom two layers contain all of the routing for the output phase current, as it leaves each half-bridge through vias, then travels along wide polygons on both copper layers to the XENSIV™ Hall effect current sensors. The phase current continues to the other side of the sensor, following the same path through wide polygons on both layers until reaching the output terminals. The shapes of polygons on these two layers are matched exactly to avoid stray capacitance to DC power or signal copper at the edges of the shapes. There is some horizontal capacitive coupling at the perimeter of the shapes, but this is quite low due to the small cross-sectional area of the copper edges. When necessary, it can be further minimized by widening the creepage rules around switch-node polygons.

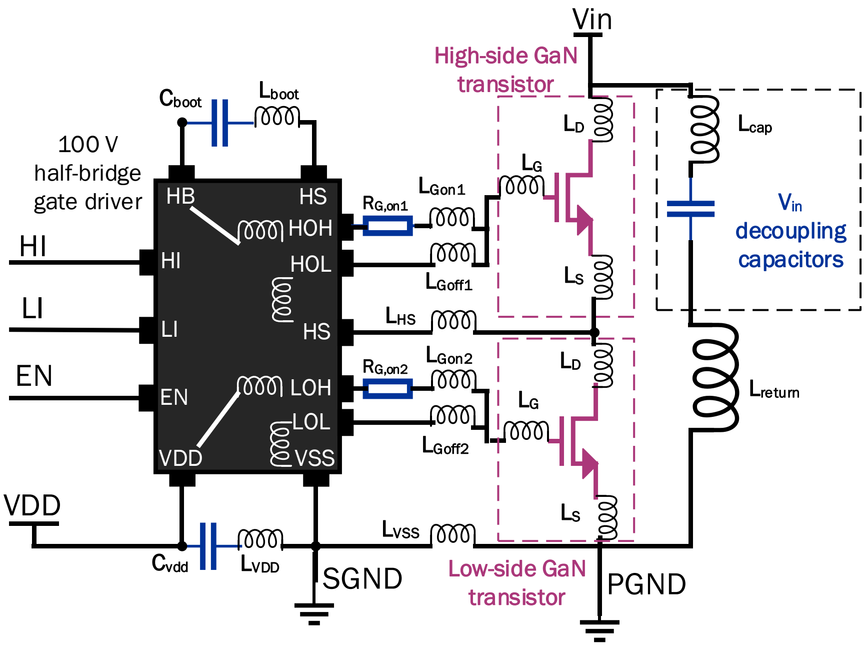
The remaining area on these bottom two layers contains all signal routing and signal ground (SGND) shielding. In systems with only one ground net, this copper can also support the top two layers routing PGND current, but then it is very important to manage the positions of bulk capacitors and decoupling capacitors to avoid ground bounce or noise coupling in the vicinity of signal routing. Regarding the parallel copper between the inner two layers, mid-layer 1, and mid-layer 2, It is unavoidable for some overlap to occur in the board, but here the dielectric thickness between the two copper layers is ~1 mm. In designs with many more layers, the cores/prepregs between layers pairs will likely be thinner for manufacturability reasons, and then it can become more difficult to minimize the overlaps. One approach is to group all switching copper area into adjacent layers, rather than alternating them across the layer stack.

## 3.3 Overview of switching commutation loops

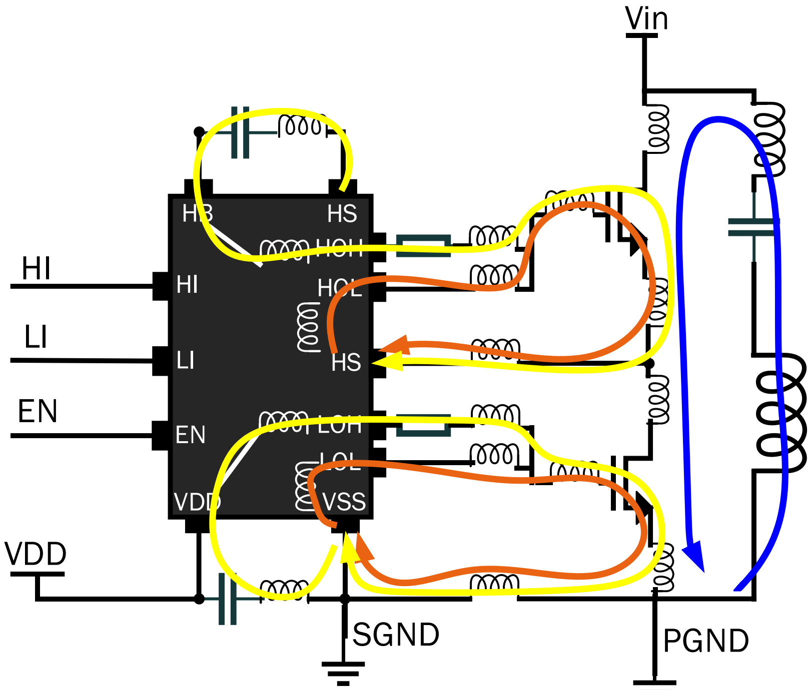
The primary goal of CoolGaN™ BDS half-bridge layout is to minimize the switching commutation loops. These loops contain inductances that result in drain voltage overshoot, gate voltage overshoot, and spurious switching events. Figure 6 shows a simplified schematic of a half-bridge. Part (a) indicates some of the lumped inductances within the components and between them, while (b) highlights the displacement current paths involved in turn-on and turn-off transitions.

Whenever the drain voltage swings to VIN or PGND, charges must be displaced between $C_{OSS,Q1}$ and $C_{OSS,Q2}$, as one VDS rises and the other falls. The displacement current follows the path marked with a blue arrow, flowing between the two transistors and the nearest VIN decoupling capacitors. CoolGaN™ BDS come in an ultra-low-inductance package with the dominant inductances in this loop come from the decoupling capacitors and the return loop that connects the components together.

Similar loops are followed whenever a gate voltage rises to turn on the transistor, as marked with yellow arrows in Figure 6(b). However, when the gate voltage is falling to turn off a transistor, this loop is slightly different. During a gate turn-off, the gate charge $Q_G$ is removed from the gate and dissipated passively as by the driver IC. Therefore, the turn-off gate loop does not contain any capacitors, as shown with orange arrows (Figure 6(b)). In a turn-on transition, the driver moves charge into the gate, so this loop must contain a capacitor to supply the charge.



(a) Annotated with the parasitic inductances inserted into power loop and gate loops



(b) With the power loop indicated in blue, turn-on (source) gate loops indicated in yellow, and turn-off (sink) gate loops indicated in orange

**Figure 6** **Simplified representation of a GaN half-bridge circuit with a half-bridge gate driver**

The power loop is mostly independent of the gate loops. However, from Figure 6 that the inductances labeled $L_S$ are shared between the power loop and gate loops. This common-source inductance can be very small, but it can become problematic if not managed well. A high common-source inductance generally has the same effect as a large gate resistor, slowing down the turn-on and turn-off transitions and causing additional switching loss.

## 3.4 Minimizing loop inductances with first inner layer return

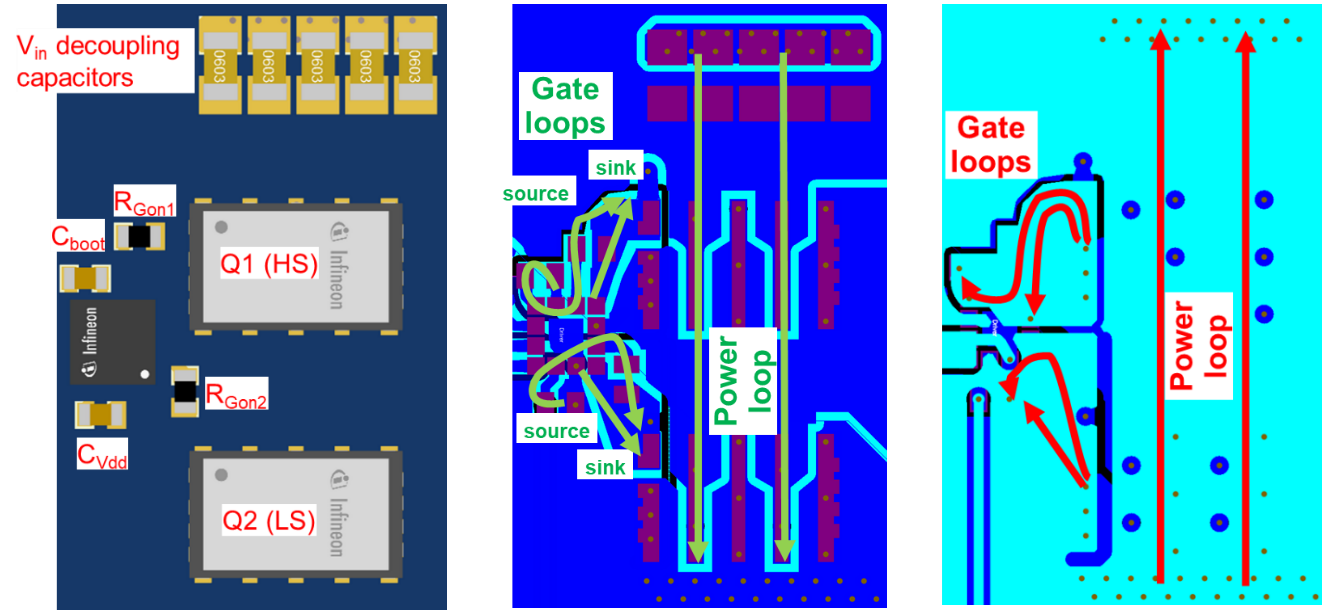
The “first inner layer return” PCB layout technique has already been embraced by much of the power electronics community, especially when it comes to GaN, SiC, or even the latest state-of-the-art Si MOSFETs [3], [4], and [5]. This technique uses magnetic field cancellation to minimize all of the inductances shown in Figure 6, while also containing the high-frequency current to a tight area to limit unwanted coupling.

Figure 7 and Figure 8 show two examples of this layout, implemented with a level-shifted half-bridge gate driver and with single-channel high-side drivers, respectively. In each figure, the green arrows indicate half of each loop shown in Figure 8, and the red arrows show the other half of each loop. Each loop is split between the top copper layer and the first inner layer, with vias located to allow for the current path on the inner layer to mirror the path on the top. The shielding polygons on this inner layer are sometimes described as “image planes,” where the current path of the top layer is projected down to the polygon below, even if there are more direct routes for the current to flow between vias on the inner layer.

Also, it is important to consider the separation of the power loop and gate loops to limit common-source inductance and avoid unwanted side-effects that can result from it. This separation can be accomplished in several ways. The main method is simple geometry. Whenever possible, the gate loops should be routed perpendicular to the power loop, as shown in Figure 8. To further reinforce this separation, a separate PGND island provides the low-side gate return. The geometrical approach is more difficult with half-bridge drivers, where the gate loop must run somewhat in parallel to the power loop due to the position of the driver. In Figure 7, a vertical slit is cut out from the PGND polygon to separate the gate and power loop returns, only in the area where the two loops run nearly parallel. It is optional to completely island this gate shield, or to navigate the issue with careful use of geometry and cutouts. Either approach can ensure low common-source inductance for the low-side gate loop where it flows on mid-layer 1.

With proper implementation of this technique, the connections of gate loops and power loops on other PCB layers are less critical. Any commutation loops beyond the first inner layer are in parallel to the lowest inductance/impedance path and therefore will conduct very little switching current. In the same way, it is usually fine to allow lateral power loops or gate loops to be present on the top layer. As long as there exists a lower-inductance path parallel with the first inner layer return, these other loops will only support the conduction of low-frequency power currents and not play a major role in the switching commutations. This is especially helpful for routing the first source pad, the shortest source pad positioned next to the gate. CoolGaN™ BDS does not require a Kelvin source because the inductances inside the package are so low. However, this first source pad is mainly used as a gate loop return on the first inner layer. On the top layer and all other layers, the pad and its related vias can be connected elsewhere for power flow. This approach mitigates common-source inductance without cutting off that source pad from the flow of steady-state current.

The placement and types of vias are also important considerations here. When possible, vias-in-pad are an excellent way to shrink commutation loops and also conduct heat and power to large copper polygons on other layers of the PCB. When within a pad, the via must normally be filled with conductive material or non-conductive epoxy, to prevent solder paste from leaking through. This manufacturing process is more expensive than standard vias. Therefore, when filled vias are too costly, it is also reasonable to place the vias nearby to the components, without being directly within the pads. This increases the inductance in critical loops, but it can be an acceptable compromise when unavoidable. When vias cannot be placed in pads, it is advisable to increase the distance between the high-side and low-side transistors to allow an open alley for phase-node current to travel to the load, and also for a less congested heat gradient around each transistor.

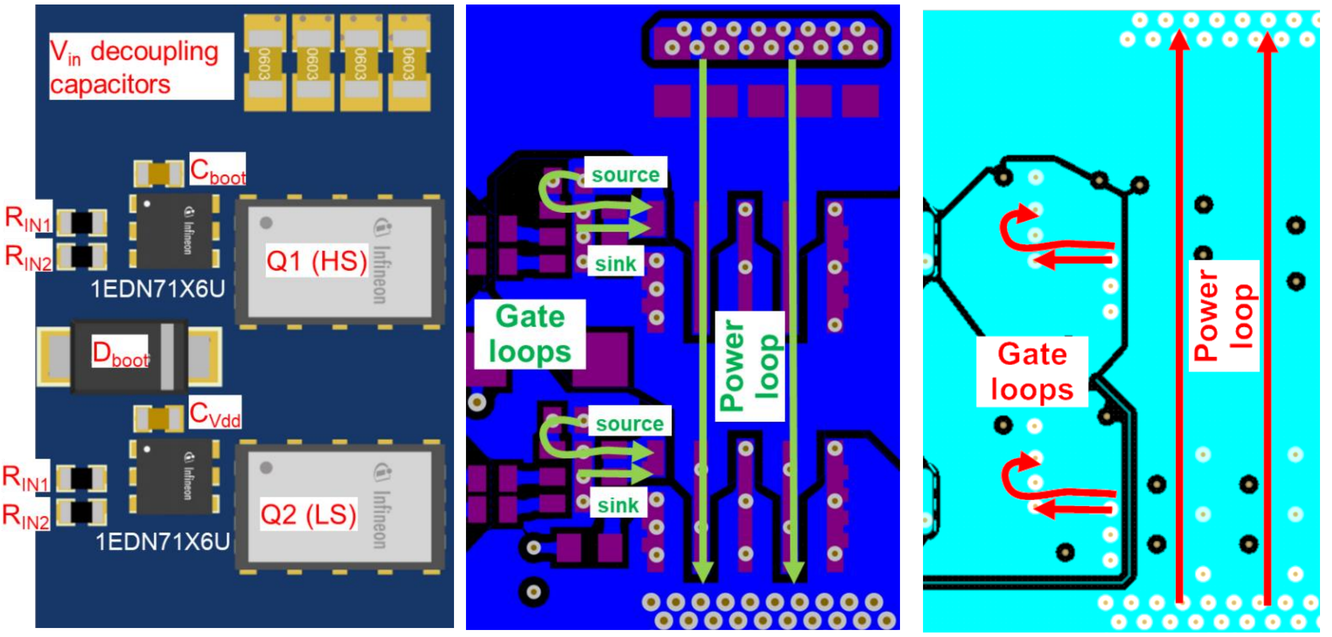


(a) Top view of board

(b) Top copper layer with components pads marked in purpose and displacement loop positive paths marked in green

(c) Mid-layer 1 with displacement loop return paths marked in red

**Figure 7** **Half-bridge layout for CoolGaN™ in 3 mm × 5 mm PQFN package using half-bridge gate driver from the EiceDRIVER™ 2EDL501xxx-U2D family**



(a) Top view of board

(b) Top copper layer with components pads marked in purpose and displacement loop positive paths marked in green

(c) Mid-layer 1, with displacement loop return paths marked in red

**Figure 8** **Half-bridge layout for CoolGaN™ in 3 mm × 5 mm PQFN package using single-channel TDI gate drivers from the EiceDRIVER™ 1EDN71x6U family**

When vias-in-pad are used, it is also important to avoid the “Swiss cheese effect” that occurs when the first inner layer is interrupted by too many via holes. For example, in Figure 7 and Figure 8, the first inner layer return is used for the PGND net on the low-side source. However, there are several switch-node vias beneath the low-side and high-side transistors, and these vias create gaps in the PGND return on the first inner layer. As long as there is significant copper below the transistors for the return current to flow, this usually causes minimal increase in the loop inductance. However, the “Remove unused pad shapes” tool can be used in the PCB design software to eliminate annular rings around vias on layers where they do not connect to other objects. This tool allows for the polygons to repour closer to the via hole and is a helpful option to mitigate the “Swiss cheese effect.”

There are instances where the gate drivers cannot fit on the same side of the PCB as the transistors due to space constraints. It is possible to locate the driver on the opposite side of the board using the same approach. The gate loop inductances will be higher, but proper shielding makes a significant difference. The entire driving circuit should be on the side with the driver, especially the low-side and high-side decoupling capacitors. The gate resistor can optionally be next to the driver or next to the transistor’s gate pad. In this case, the gate shielding islands must be positioned in the inner layer below the driving circuit, rather than below the transistors.

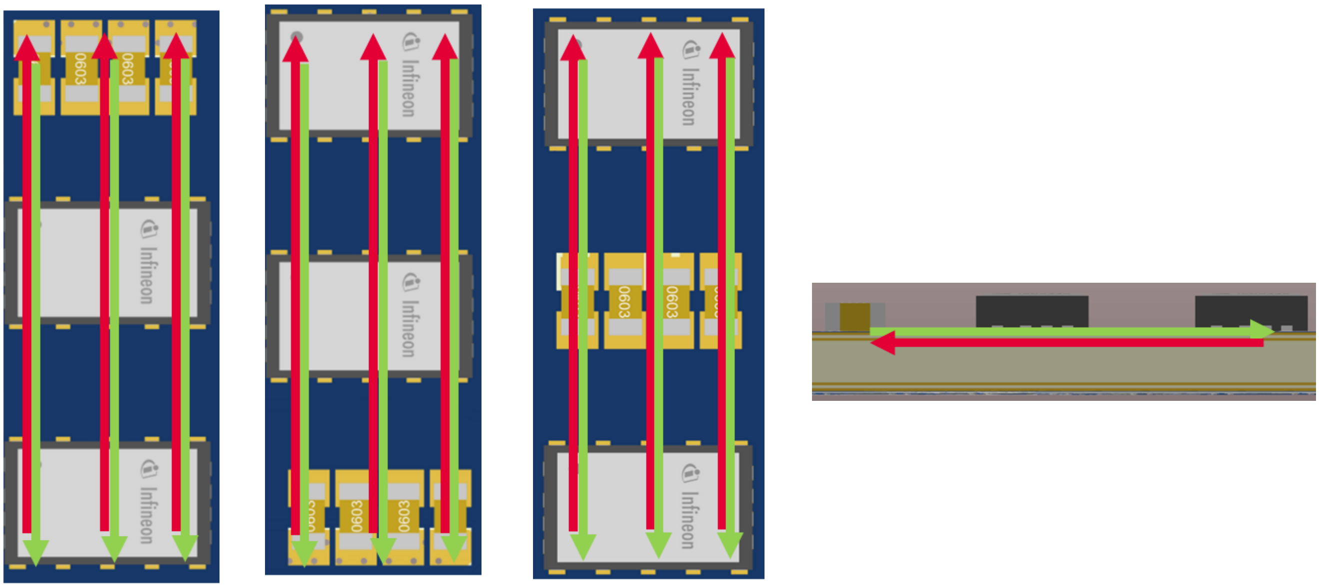
## 3.5 Power loop layout options

The first inner layer return is a basic framework for half-bridge layout. It is not a one-size-fits-all solution. This section will show some variations of the implementations in Figure 7 and Figure 8 that can also work well, and explain why some variations are not recommended.

Figure 9 shows three options for an optimal return for the power loop, while the gate driving circuit layout remains similar to the previous section. Part (a) is the same layout as shown in Figure 7 and Figure 8, where the

PGND net (low-side source) is used to close the power loop on the first inner layer. Part (b) repositions the decoupling capacitors near the low-side source and uses the $V_{IN}$ net (high-side drain) to close the loop. Part (c) moves the capacitors between the two transistors, and here the switch-node is used as the loop return. All three of these options result in the same cross-sectional loop area depicted in part (d). The low inductance comes from the tight spacing between these two layers, the length of the path on both layers, and the width of the loop (i.e., the number of parallel arrows that can be drawn in the diagram). For example, with 80 µm dielectric thickness, the cross-sectional area is ~1 $mm^2$, the width is ~4 mm, and the loop inductance is ~400 pH.

Figure 9 shows two commonly implemented alternatives, the vertical two-sided loop (a), and the lateral loop (b). These two half-bridges result in significantly higher power loop inductance. It is understood from examination of the loop areas and widths in the figure. The path length for the vertical loop looks shorter, but the loop area now crosses the full thickness of the PCB. With a 1.4 mm thick PCB, the cross-sectional area is now 4 $mm^2$ for the tightest loop, and 13 $mm^2$ for the widest loop. The lateral loop has a similar issue. The tightest loop is only 2 $mm^2$ in area, while the widest loop is 30 $mm^2$. The high-frequency displacement current is likely to favor the smaller 2 $mm^2$ loop area, but this means that the loop width is very small, likely <1 mm. Both of these layouts exceed 1 nH in power loop inductance. Furthermore, it is more challenging to geometrically decouple the gate loops from the power loop in the lateral implementation. See [6] and [7] for detailed explanation of power loop design for multiple GaN switches connected in parallel.



(a) GND return

(b) VIN return

(c) SW return

(d) cross-sectional view of GND return to visualize the loop area

**Figure 9** **Recommended half-bridge layout for CoolGaN™ in 3 mm × 5 mm PQFN package showing three options for first-inner-layer return**

# 4 Related resources

- Gallium nitride (GaN) webpage
- GaN developer community

## References

[1] Infineon Technologies AG (formerly GaN Systems): *Design considerations of paralleled GaN-based half bridge power stage*; Available online

[2] Infineon Technologies AG: *AN_2210, Innovative dual-side cooled 5 x 6 PQFN package,* 2022; Available online

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# Glossary

**BDS**
*bidirectional switch (BDS)*

**GaN**
*gallium nitride (GaN)*

**HB**
*half-bridge (HB)*

**PQFN**
*power quad flat no-lead (PQFN)*

**SiC**
*silicon carbide*

**SR**
*synchronous rectifier (SR)*

**TIM**
*thermal interface material (TIM)*

**ZVT**
*zero voltage turn-on (ZVT)*

## Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| V 1.0 | 2025-08-21 | Initial release |

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